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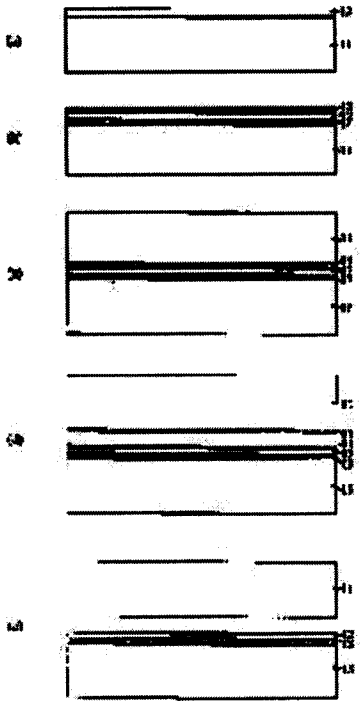
(54) MANUFACTURING METHOD OF SEMICONDUCTOR MEMBER

(57)Abstract:

PROBLEM TO BE SOLVED: To realize a semiconductor member of high quality, by sticking together a first substrate and a second substrate, so as to obtain a multilayered structure wherein non-porous semiconductor layers are positioned inside, isolating the multilayered structured body by an ion implanted layer, and eliminating the ion implanted layer left on the isolated second substrate.

SOLUTION: A non-porous semiconductor layer 12 is formed on a first substrate 11. Ions are implanted in the vicinity of the interface of the layer 12 and the substrate 11 or in the layer 12, thereby forming an ion puddle 14. The first substrate 11 and the second substrate 15 are stuck together via an insulating layer 13, so as to obtain a multilayered structure body. By using the ion puddle 14, the multilayered structure body is isolated. The ion puddle 14 left on the isolated second substrate 15 is eliminated. The surface is flattened, and the substrates are again used as the first substrate 11 or the substrate 15. As a result, a semiconductor member of high quality can be realized at a low cost.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The process which prepares the 1st base which has the ion-implantation layer of the nonvesicular semi-conductor layer allotted on the silicon substrate and this silicon substrate, said silicon substrate, or said nonvesicular semi-conductor layer formed in either at least, The process which sticks said the 1st base and 2nd base so that the multilayer-structure object with which said nonvesicular semi-conductor layer is located inside may be acquired, The manufacture approach of the semi-conductor member characterized by having the process which separates said multilayer-structure object in said ion-implantation layer, and the process which removes the ion-implantation layer which remained in said separated 2nd base side.
[Claim 2] The process which prepares the 1st base which has the ion-implantation layer of the nonvesicular semi-conductor layer allotted on the silicon substrate and this silicon substrate, said silicon substrate, or said nonvesicular semi-conductor layer formed in either at least, The process which sticks said the 1st base and 2nd base so that the multilayer-structure object with which said nonvesicular semi-conductor layer is located inside may be acquired, The process which separates said multilayer-structure object in said ion-implantation layer, the process which removes the ion-implantation layer which remained in said separated 2nd base side, The manufacture approach of the semi-conductor member characterized by having the process which uses the base which removes the ion-implantation layer which remained in said separated 1st base side, and is obtained as a raw material of said 1st base.
[Claim 3] The process which prepares the 1st base which has the ion-implantation layer of the nonvesicular semi-conductor layer allotted on the silicon substrate and this silicon substrate, said silicon substrate, or said nonvesicular semi-conductor layer formed in either at least, The process which sticks said the 1st base and 2nd base so that the multilayer-structure object with which said nonvesicular semi-conductor layer is located inside may be acquired, The process which separates said multilayer-structure object in said ion-implantation layer, the process which removes the ion-implantation layer which remained in said separated 2nd base side, The manufacture approach of the semi-conductor member characterized by having the process which uses the base which removes the ion-implantation layer which remained in said separated 1st base side, and is obtained as a raw material of said 2nd base.
[Claim 4] Said ion-implantation layer is the manufacture approach of the semi-conductor member according to claim 1 to 3 formed after forming said nonvesicular semi-conductor layer on said silicon substrate.
[Claim 5] Said ion-implantation layer is the manufacture approach of the semi-conductor member according to claim 1 to 3 formed after forming said nonvesicular semi-conductor layer on said silicon substrate, and forming an insulator layer on this nonvesicular semi-conductor layer further.
[Claim 6] Said ion-implantation layer is the manufacture approach of the semi-conductor member according to claim 1 to 3 formed using the ion which consists of an element chosen from rare gas, hydrogen, and nitrogen.
[Claim 7] The injection rate of said ion is 1016-1017-/cm2. The manufacture approach of the semi-conductor member according to claim 6 controlled by the range.

[Claim 8] The thickness of said ion-implantation layer is the manufacture approach of the semi-conductor member according to claim 1 to 3 controlled by 500A or less.
[Claim 9] The thickness of said ion-implantation layer is the manufacture approach of the semi-conductor member according to claim 8 controlled by 200A or less.
[Claim 10] Separation of said multilayer-structure object is the manufacture approach of the semi-conductor member according to claim 1 to 3 made by applying the force to said ion-implantation layer from the exterior.
[Claim 11] The approach of applying said force is the manufacture approach of the semi-conductor member according to claim 10 chosen from pressurizing in the direction perpendicular to said base front face, pulling in the direction perpendicular to a base front face, and applying shearing force.
[Claim 12] Separation of said multilayer-structure object is the manufacture approach of the semi-conductor member according to claim 1 to 3 performed by oxidizing this lamination ****** after making an ion-implantation layer express at the edge of said multilayer-structure object.
[Claim 13] Separation of said multilayer-structure object is the manufacture approach of the semi-conductor member according to claim 1 to 3 made by heating this multilayer-structure object.
[Claim 14] The manufacture approach of a semi-conductor member according to claim 13 that said heating is what heats said whole multilayer-structure object.
[Claim 15] The manufacture approach of a semi-conductor member according to claim 13 that said heating is what heats said multilayer-structure object partially.
[Claim 16] The manufacture approach of a semi-conductor member according to claim 15 that said heating is made by laser radiation.
[Claim 17] Said laser is the manufacture approach of the semi-conductor member according to claim 16 which is carbon dioxide laser.
[Claim 18] The manufacture approach of a semi-conductor member according to claim 15 that said heating is made by passing a current in said ion-implantation layer.
[Claim 19] The manufacture approach of a semi-conductor member according to claim 1 to 3 that said nonvesicular semi-conductor layer consists of single-crystal-silicon layers.
[Claim 20] Said single-crystal-silicon layer is the manufacture approach of the semi-conductor member according to claim 19 formed of epitaxial growth.
[Claim 21] The manufacture approach of the semi-conductor member according to claim 19 which a silicon oxide layer is formed in the front face of said single-crystal-silicon layer, and constitutes said 1st base.
[Claim 22] Said silicon oxide layer is the manufacture approach of the semi-conductor member according to claim 21 formed of thermal oxidation.
[Claim 23] The manufacture approach of a semi-conductor member according to claim 1 to 3 that said nonvesicular semi-conductor layer consists of compound semiconductor layers.
[Claim 24] The manufacture approach of a semi-conductor member according to claim 23 that said compound semiconductor layer constitutes a single crystal.
[Claim 25] The manufacture approach of the semi-conductor member according to claim 1 to 3 using a single crystal silicon substrate as said 2nd base.
[Claim 26] The manufacture approach of the semi-conductor member according to claim 1 to 3 using the substrate which formed the oxide film in the front face of a single crystal silicon substrate as said 2nd base.
[Claim 27] The manufacture approach of the semi-conductor member according to claim 1 to 3 using a light transmission nature base as said 2nd base.
[Claim 28] The manufacture approach of a semi-conductor member according to claim 27 of using a glass substrate for said light transmission nature base.
[Claim 29] Said lamination process is the manufacture approach of the semi-conductor member according to claim 1 to 3 made by sticking two bases.
[Claim 30] Said lamination process is the manufacture approach of the semi-conductor member according to claim 1 to 3 made using anode plate junction, pressurization, and heat treatment.

[Claim 31] Removal of said ion-implantation layer is the manufacture approach of the semi-conductor member according to claim 1 to 3 made by polish.
[Claim 32] Removal of said ion-implantation layer is the manufacture approach of the semi-conductor member according to claim 1 to 3 made by etching.
[Claim 33] Said etching is the manufacture approach of the semi-conductor member according to claim 32 made using fluoric acid.
[Claim 34] The semi-conductor member manufactured by the approach according to claim 1 to 33.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of a semi-conductor member including the process which transfers especially a semi-conductor layer on another base (transfer) about the manufacture approach of the semi-conductor member for forming semiconductor devices, such as a semiconductor integrated circuit, and a solar battery, semiconductor laser, light emitting diode.
[0002]
[Description of the Prior Art] The semi-conductor member shall be known under the name of the semi-conductor wafer, the semi-conductor substrate, the semiconductor device, etc., and shall contain that in which the semiconductor device is formed using the semiconductor region, and the thing of the condition before a semiconductor device is formed.
[0003] In such a semi-conductor member, some which have a semi-conductor layer are in an insulating lifter.
[0004] Formation of the single crystal Si semi-conductor layer of an insulating lifter is silicon. ON It was widely known as an insulator (SOI) technique, and in the bulk Si substrate which produces the usual Si integrated circuit, since the device using a SOI technique has many dominance points which cannot reach, many researches have accomplished. that is, 3. stray capacity which 1. dielectric separation is easy for, and is excellent in the possibility of high integration and 2. opposite radiation resistance using a SOI technique decreases -- having -- the possibility of improvement in the speed, and 4. -- a well -- the possibility of the perfect depletion mold field-effect transistor by the formation of 6. thin film which can prevent 5. latch rise which can skip a process, and the dominance point of ** are acquired. These are detailed in the following reference. SpecialIssue: "Single-crystal silicon on non-single-crystal insulators";edited by G.W.Cullen, Journal of Crystal Growth, volume 63 no 3 pp 429-590 (1983).
[0005] Furthermore in the past several years, many reports are made as a substrate with which SOI realizes improvement in the speed of MOSFET, and low-power-ization (IEEE SOI conference 1994). Moreover, since an insulating layer is in the lower part of a component when SOI structure is used, as a result of being able to simplify an isolation process compared with the case where a component is formed on a bulk Si wafer, a device process process is shortened. That is, together with high-performance-izing, low-pricing in total of wafer cost and process cost is expected compared with MOSFET on bulk Si, and IC.
[0006] Improvement in the speed according [the perfect depletion mold MOSFET] to improvement in driving force and low-power-ization are expected especially. Although the threshold voltage (Vth) of MOSFET is generally determined by the high impurity concentration of the channel section, in the case of the perfect depletion mold (FD;FullyDepleted) MOSFET using SOI, depletion-layer thickness will be influenced of the thickness of SOI. Therefore, in order to build a large-scale integrated circuit with the sufficient yield, homogeneity of SOI thickness was desired strongly.
[0007] Moreover, the device on a compound semiconductor has in Si the high engine performance which is not obtained, for example, a high speed, luminescence, etc. Most of these devices carries out

epitaxial growth on compound semiconductor substrates, such as GaAs, and current is made in it. However, a compound semiconductor substrate is expensive, a mechanical strength is low, and a large area wafer has which trouble with difficult production.

[0008] From such a thing, it is cheap, and a mechanical strength is also high and the attempt which carries out heteroepitaxial growth of the compound semiconductor on Si wafer which can produce a large area wafer is made.

[0009] The research on formation of a SOI substrate was prosperous from around the 1970s. In early stages, the approach (SOS:Sapphire on Silicon) of carrying out heteroepitaxial growth of the single crystal Si on the silicon on sapphire which is an insulating material, the approach (FIPOS:Fully Isolation by Porous Oxidized Silicon) of forming SOI structure according to the dielectric separation by oxidation of Porosity Si, and oxygen ion-implantation were often studied.

[0010] The FIPOS method is the approach of carrying out dielectric separation of the N type Si island by accelerating oxidation, after porosity-izing only a P type Si substrate by the anodization method in HF solution so that an N type Si layer may be formed in a P type Si single crystal substrate front face at island shape by the proton ion implantation, (J.Crystal Growth besides Imai, vol 63,547) (1983), or epitaxial growth and patterning and Si island may be surrounded from a front face. By this approach, Si field separated is determined before the device process, and there is a trouble that the degree of freedom of a device design may be restricted.

[0011] Oxidation ion-implantation is an approach called SIMOX reported for the first time by KIzumi. It is 1017-1018-/cm2 about oxygen ion to Si wafer. After carrying out extent impregnation, it anneals at the elevated temperature of about 1320 degrees in an argon and an oxygen ambient atmosphere. Consequently, the oxygen ion poured in focusing on the depth equivalent to the projection range (Rp) of an ion implantation combines with Si, and an oxidation Si layer is formed. In that case, Si layer made amorphous by the oxygen ion implantation of the upper part of an oxidation Si layer is also recrystallized, and it becomes a single crystal Si layer. the defect included in surface Si layer -- conventional 105 / cm2 although many -- the amount of placing of oxygen -- 4x1017-/cm2 carrying out near -- it is -102 / cm2 up to -- it has succeeded in decreasing. However, since the range of the impregnation energy which can maintain the crystallinity of the membraneous quality of an oxidation Si layer and a surface Si layer etc., and an injection rate was narrow, the thickness of a surface Si layer and an embedding oxidation Si layer (BOX;Burried Oxide) was restricted to the specific value. In order to obtain the surface Si layer of desired thickness, sacrifice oxidation or to grow epitaxially were required. In that case, as a result of being superimposed on the degraded minute by these processes, there is a trouble that thickness homogeneity deteriorates in distribution of thickness.

[0012] Moreover, it is reported that the poor formation field of Oxidation Si where SIMOX is called a pipe exists. As one of the cause of this, foreign matters, such as dust at the time of impregnation, are considered. In the part in which a pipe exists, degradation of a device property will arise by leak between a barrier layer and a support substrate.

[0013] As the above-mentioned [the ion implantation of SIMOX], since there are many injection rates compared with the ion implantation used in the usual semi-conductor process, even if the equipment of dedication is developed, in addition, impregnation time amount is long. Since an ion implantation carries out the raster scan of the ion beam of the predetermined amount of currents, or extends a beam and is performed, increase of impregnation time amount is assumed with large-area-izing of a wafer. Moreover, in elevated-temperature heat treatment of a large area wafer, it is pointed out that problems, such as generating of the slip by the temperature distribution in a wafer, become severeer. In SIMOX, in Si semi-conductor process of 1320 degrees C, since the elevated temperature which is not usually used needs to be heat-treated, we are anxious about the importance of this problem becoming still larger including equipment development.

[0014] Moreover, apart from the formation approach of the above conventional SOI, the approach of using heat treatment or adhesives for another Si single crystal substrate which oxidized Si single crystal substrate thermally, and forming lamination and SOI structure is capturing the spotlight in recent years. This approach needs to thin-film-ize the barrier layer for a device to homogeneity. That is, it is

necessary to thin-film-ize Si single crystal substrate with a thickness of hundreds of micrometers less than [mum order or it]. There are three kinds of approaches in this thin film-ization as follows.
(1) It is difficult to thin-film-ize to homogeneity in the polish of thin-film-izing (1) by the thin film-ized (3). selective etching by thin film-ized (2). partial plasma etching by . polish. Especially as for thin film-ization of sub mum, dispersion also becomes dozens of% and this equalization poses a big problem. If diameter-ization of macrostomia of a wafer furthermore progresses, whenever [the / difficult] will just increase.
[0015] After thin-film-izing the approach of (2) by the approach by polish of (1) to about 1-3 micrometers by the approach of (1) beforehand, it carries out multipoint measurement of the thickness distribution on the whole surface. next -- this thickness distribution -- being based -- SF6 with a diameter of several mm etc. -- it etches amending thickness distribution by making the used plasma scan, and thin-film-izes to desired thickness. By this approach, it is reported that thickness distribution is made to about **10mm. However, since this foreign matter will serve as an etching mask if there is a substrate top foreign matter (particle) in the case of plasma etching, a projection will be formed on a substrate.
[0016] Moreover, since the front face is ruined immediately after etching, touch polishing is required after plasma-etching termination, but since control of the amount of polishing is performed by time management, control of the last thickness and degradation of the thickness distribution by polishing are pointed out. Since abrasive materials, such as colloidal silica, furthermore grind the front face which becomes a barrier layer directly against polish, we are anxious also about formation of the crushing layer by polish, and installation of processing distortion. Since plasma-etching time amount increases in proportion to increase of wafer area when a wafer is furthermore large-area-ized, we are anxious also about the remarkable fall of a throughput.
[0017] The approach of (3) is the approach of building the film configuration in which selective etching is possible to the substrate thin-film-ized beforehand. For example, it is 1019-/cm3 about boron on a P type substrate. The laminating of the thin layer of P+-Si and the thin layer of P type Si which were included in the above concentration is carried out by approaches, such as epitaxial growth, and it considers as the 1st substrate. After sticking this with the 2nd substrate through insulating layers, such as an oxide film, the rear face of the 1st substrate is beforehand made thin by grinding and polish. Then, it is P+ by the selective etching of a P type layer. It is a layer to exposure and a pan P+ A P type layer is exposed by the selective etching of a layer, and SOI structure is completed. This approach is detailed to the report of Maszara (W. P.Maszara, J.Electrochem.Soc., vol.138,341 (1991)).
[0018] although selective etching is effective in uniform thin-film-izing - at most 102 A selection ratio is not enough.
[0019] - Since the front-face nature after etching is bad, a touch polish is needed after etching. However, while thickness decreases as a result, thickness homogeneity also tends to deteriorate. Although especially polishing manages the amount of polishes by time amount, since dispersion in a polish rate is large, control of the amount of polishes is difficult. Therefore, in formation of an ultra-thin SOI layer, such as 100nm, it becomes especially a problem.
[0020] - Since the epitaxial growth or heteroepitaxial growth on an ion implantation and a high concentration B dope Si layer is used, the crystallinity of a SOI layer is bad. Moreover, the front-face nature of a lamination-ed side is also inferior to the usual Si wafer.
there is a trouble of ** (C. -- Harendt, et.al., and J.Elect.Mater.Vol.20,267 (1991) --) H. Baumgart, et.al.Extended Abstract of ECS 1st International Symposium of Wafer Bonding, pp-733 (1991), C. E.Hunt, Extended Abstract of ECS 1st International Symposium of Wafer Bonding, pp-696 (1991). Moreover, it depends for the selectivity of selective etching on the concentration difference and the steepness of the depth direction profile of impurities, such as boron, greatly. Therefore, if hot epitaxial growth is performed in order to raise hot bonding annealing for raising lamination reinforcement, and crystallinity, the depth direction distribution of high impurity concentration will spread, and the selectivity of etching will deteriorate. That is, coexistence of improvement in lamination reinforcement was difficult for the crystallinity of improvement in the selection ratio of etching.

[0021] Meanwhile, these people proposed the manufacture approach of a new semi-conductor member in JP,5-21338,A previously. The approach indicated by the official report concerned is a thing as follows. That is, after it forms the member which allotted the nonvesicular single crystal semiconductor region on a porosity single crystal semiconductor region and a front face sticks the front face of the member which consisted of insulating matter on the front face of said nonvesicular single crystal semiconductor region, it is the manufacture approach of the semi-conductor member characterized by removing said porosity single crystal semiconductor region by etching.
[0022] Moreover, Maibara and others which is the artificer of this invention was excellent in thickness homogeneity or crystallinity, and reported lamination SOI in which batch processing is possible (64 T. Yonehara et.al., Appl.Phys.Lett.vol. 2108 (1994)). Hereafter, the production approach of this lamination SOI is explained using drawing 4 (a) - (c).
[0023] By this approach, the porous layer 42 on the Si substrate 41 is used as an ingredient which performs selective etching. On a porous layer 42, the nonvesicular single crystal Si layer 43 is stuck with the 2nd substrate 44 through the oxidation Si layer 45, after growing epitaxially (drawing 4 (a)). Lamination of the 1st substrate is carried out by approaches, such as polish, from a rear face, and Porosity Si is exposed on the whole substrate surface (drawing 4 (b)). the exposed porosity Si -- KOH and HF+H 2O2 etc. -- it etches with a selection etching reagent and removes (drawing 4 (c)). Since the selection ratio of etching to the bulk Si of Porosity Si (nonvesicular single crystal Si) can be made high enough with 100,000 times at this time, the nonvesicular single crystal Si layer which grew on porosity beforehand can be transferred on the 2nd substrate, without reducing most thickness (transfer), and a SOI substrate can be formed. Therefore, the thickness homogeneity of SOI is mostly determined at the time of epitaxial growth. Since epitaxial growth can use the CVD system usually used in a semi-conductor process, as for the homogeneity, according to Sato's and others report (SSDM95), less than [100nm**2%] is realized. Moreover, the crystallinity of an epitaxial Si layer is also good and they are 3.5x102 / cm2. It was reported.
[0024] By the conventional approach, since the selectivity of etching was based on the difference and the profile of the depth direction of high impurity concentration, the temperature (lamination, epitaxial growth, oxidation, etc.) of heat treatment which extends concentration distribution was greatly restrained in general with 800 degrees C or less. On the other hand, since etching in this approach has determined the rate of etching of the difference of the structure of porosity and bulk, it is reported that constraint of heat treatment temperature is small and heat treatment of about 1180 degrees C is possible. For example, heat treatment after lamination raises the bond strength of wafers, and decreasing the number of the openings (void) produced in a lamination interface and magnitude is known. moreover, ** -- by etching based on a structure difference [like], even if there is particle which adhered on Porosity Si, thickness homogeneity is not affected.
[0025] However, the semi-conductor substrate using lamination surely needs two wafers, most is almost vainly removed by polish, etching, etc., one sheet is thrown away, and the resource of the limited earth is [among those] useless [a sheet]. Therefore, in SOI by lamination, the controllability, the homogeneous formation of other low cost, and improvement in economical efficiency are just going to desire.
[0026] That is, coincidence was expected saving resources by the reuse of a wafer etc., and the method of realizing a cost cut while quality produced enough SOI substrates with sufficient repeatability.
[0027] Meanwhile, after these people stuck two substrates previously, they separated the stuck substrate in the porous layer, removed residual porosity from one substrate after separation, and proposed the manufacture approach of the semi-conductor substrate which reuses this substrate by JP,7-302889,A. Drawing 5 (a) - (c) is used for below, and one example of the approach indicated by the official report concerned is explained to it.
[0028] After porosity-izing the surface layer of the 1st Si substrate 51 and forming a porous layer 52, the single crystal Si layer 53 is formed on it, and the principal plane of 2nd Si substrate 54 with another this single crystal Si layer and 1st Si base is stuck through an insulating layer 55 (drawing 5 (a)). Then, a SOI substrate is formed by dividing the wafer stuck by the porous layer (drawing 5 (b)), and removing

alternatively the porosity Si layer exposed to the front face by the side of 2nd Si base (drawing 5 (c)). The 1st substrate 41 can remove and reuse the porous layer which remained.
[0029] Invention indicated by JP,7-302889,A is very useful when attaining low cost-ization of a semi-conductor substrate, since the substrate with which the structure of a porosity silicon layer dissociates and used the substrate for the making process of a semi-conductor substrate once using the brittle point compared with nonvesicular silicon can be again used for the making process of a semi-conductor substrate.
[0030] Independently, after forming the semi-conductor layer which constitutes the photo-electric-conversion section of a solar battery on a porosity silicon layer, separating this semi-conductor layer from a porous layer is indicated by JP,8-213645,A, and it is too indicated to be this to it to reuse the substrate with which the porosity silicon layer was formed also here.
[0031] On the other hand, although a base is separated using such a porosity silicon layer, otherwise, the technique of separating a base, without using such a porosity silicon layer is indicated by JP,5-211128,A. The approach of making a bubble layer by the ion implantation in a silicon substrate, making this bubble layer producing the crystal rearrangement by heat treatment and condensation of air bubbles, and removing the field by the side of the outermost surface of a silicon substrate (called "the thin semiconductor material film" in this official report) bordering on a bubble layer is indicated by this official report. In short, the impregnation ion of the bulk Si outermost surface does not exist, or a thin semiconductor material film here is a field with very little abundance. however, to Si wafer of bulk Flow pattern defect () [FPD;Flow] Pattern Defect (T. Abe, Extended Abst.Electrochem.Soc.Spring Meeting vol.95-1, pp.596, (May, 1995)) and COP () [Crystal] Originated It is becoming clear that defects peculiar to it, such as Particles (a Hidekazu Yamamoto and "demand technical problem to diameter silicon wafer of macrostomia" 23rd ultra Clean Technology college, (Aug.1996)), exist. Therefore, a flow pattern defect and COP will exist in this thin semiconductor material film.
[0032]
[Problem(s) to be Solved by the Invention] However, if a semiconductor material film is separable from a silicon substrate in the form where such a flow pattern defect or COP do not exist, apart from the approach using the so-called porosity silicon mentioned above, a practical semi-conductor member may be able to be supplied by low cost. Then, in view of this point, this invention persons inquire and came to complete this invention.
[0033] The purpose of [purpose of invention] this invention is the manufacture approach of a semi-conductor member of having the process which sticks two bases, and is to offer the manufacture approach of the semi-conductor member which can reuse the one section of this base as a raw material of this semi-conductor member.
[0034]
[Means for Solving the Problem] The process which prepares the 1st base which has the ion-implantation layer of the nonvesicular semi-conductor layer matched with the means of this invention on the silicon substrate and this silicon substrate, said silicon substrate, or said nonvesicular semi-conductor layer formed in either at least, The process which sticks said the 1st base and 2nd base so that the multilayer-structure object with which said nonvesicular semi-conductor layer is located inside may be acquired, It is in offering the manufacture approach of the semi-conductor member characterized by having the process which separates said multilayer-structure object in said ion-implantation layer, and the process which removes the ion-implantation layer which remained in said separated 2nd base side.
[0035] The process which prepares the 1st base which has the ion-implantation layer of the nonvesicular semi-conductor layer matched with still more nearly another means of this invention on the silicon substrate and this silicon substrate, said silicon substrate, or said nonvesicular semi-conductor layer formed in either at least, The process which sticks said the 1st base and 2nd base so that the multilayer-structure object with which said nonvesicular semi-conductor layer is located inside may be acquired, The process which separates said multilayer-structure object in said ion-implantation layer, the process which removes the ion-implantation layer which remained in said separated 2nd base side, It is in the thing of the semi-conductor member characterized by having the process which uses the base which

removes the ion-implantation layer which remained in said separated 1st base side, and is obtained as a raw material of said 1st base for which the manufacture approach offer is made.
[0036] The process which prepares the 1st base which has the ion-implantation layer of the nonvesicular semi-conductor layer matched with still more nearly another means of this invention on the silicon substrate and this silicon substrate, said silicon substrate, or said nonvesicular semi-conductor layer formed in either at least, The process which sticks said the 1st base and 2nd base so that the multilayer-structure object with which said nonvesicular semi-conductor layer is located inside may be acquired, The process which separates said multilayer-structure object in said ion-implantation layer, the process which removes the ion-implantation layer which remained in said separated 2nd base side, It is in offering the manufacture approach of the semi-conductor member characterized by having the process which uses the base which removes the ion-implantation layer which remained in said separated 1st base side, and is obtained as a raw material of said 2nd base.
[0037] In the manufacture approach of the semi-conductor member of [operation] this invention, the 1st base for lamination bases is constituted using the nonvesicular semi-conductor layer allotted on the silicon substrate. A nonvesicular semi-conductor layer cannot be suitably constituted from an epitaxial semi-conductor layer, and a quality semi-conductor member can be offered from not being influenced in this case of a flow pattern defect peculiar to the above-mentioned silicon wafer, or COP (Crystal Originated Particles).
[0038] Moreover, since a nonvesicular semi-conductor layer can control an electric conduction mold and high impurity concentration easily, the manufacture approach of the semi-conductor member of this invention becomes what may satisfy various demands, and is high. [of application]
[0039] Furthermore, after separating the multilayer-structure object which sticks the 1st base and 2nd base and is acquired in an ion-implantation layer, since the silicon substrate which remained in the 1st base side is reusable as a configuration member of the 1st base or the 2nd base, it has an advantage also in respect of saving resources and low-cost-izing.
[0040] The manufacture approach of a semi-conductor member of having excelled in the field of productivity, homogeneity, a controllability, and cost when obtaining the single crystal half conductor layer excellent in crystallinity on the 2nd base which can be constituted from an insulating substrate etc. according to this invention can be offered.
[0041]
[Embodiment of the Invention] Although the suitable example of an embodiment of this invention is described hereafter, this invention is not limited to these examples of an embodiment, and the purpose of this invention should just be attained.
[0042] When the ion implantation of helium or the hydrogen is carried out to a [ion-implantation layer] single crystal silicon substrate, a minute cavity (micro-cavity) with a diameter of several nm - dozens of nm is -1016 - 1017-/cm2 to the field by which the ion implantation was carried out. Being able to form by the thing consistency, this silicon substrate serves as structure which formed the porous layer in the interior. Usable ion consists of an element chosen from rare gas, hydrogen, and nitrogen in this invention. In this invention, even if there are few nonvesicular semi-conductor layers allotted on the silicon substrate or this silicon substrate, that what is necessary is to just be formed in either, an ion-implantation layer can also be formed in both interface, and can also be formed more than two-layer. The ion injection rate of the ion-implantation layer formed by this invention is 1016-1017-/cm2, when separation of the multilayer-structure object which sticks the 1st base and 2nd base and is acquired is taken into consideration. The range is desirable. Although the thickness of an ion-implantation layer changes with acceleration voltage, when taking into consideration making into homogeneity thickness of the nonvesicular semi-conductor layer on the 2nd base obtained by generally separating 500A or less and a multilayer-structure object, it is good to consider as 200A or less preferably. The ion-implantation layer has concentration distribution in the direction of thickness, and there is an inclination for concentration distribution of an ion injection rate to be separated in respect of being the highest, in the case of separation of a multilayer-structure object.
[0043] In [nonvesicular semi-conductor layer] this invention, compound semiconductors, such as GaAs

besides a single crystal Si, Polycrystal Si, and amorphous Si, InP, GaAsP, GaAlAs, InAs, AlGaSb, InGaAs, ZnS, CdSe, CdTe, and SiGe, etc. can be suitably used as a nonvesicular semi-conductor layer. And a nonvesicular semi-conductor layer may already make semiconductor devices, such as FET (Field Efect Transistor).

[0044] In [1st base] this invention, the 1st base means the base which has the ion-implantation layer of a silicon substrate, the nonvesicular semi-conductor layer allotted on this silicon substrate, and a silicon substrate or a nonvesicular semi-conductor layer formed in either at least. Therefore, the substrate with which the 1st base formed the nonvesicular semi-conductor layer on the silicon substrate by which the ion-implantation layer was formed in the interior The thing of a rice cake theory, the thing in which insulator layers, such as a nitride and an oxide film, were formed on this nonvesicular semi-conductor layer, Or after forming an epitaxial semi-conductor layer and an insulating layer on a silicon substrate, the substrate which carried out the ion implantation to the silicon substrate, and formed the ion-implantation layer, the thing which formed the ion-implantation layer further into the nonvesicular semi-conductor layer formed on the silicon substrate are included.

[0045] In order to form a nonvesicular semi-conductor layer on a silicon substrate, a sputtering technique (a bias sputtering technique is included) besides CVD methods, such as reduced pressure CVD, plasma CVD, Light CVD, and MOCVD (Metal-Organic CVD), molecular beam epitaxy, a liquid phase grown method, etc. are employable.

[0046] As the 2nd base by which the [2nd base] nonvesicular semi-conductor layer is transferred (transfer), insulating substrates, such as what prepared insulator layers, such as an oxide film (the thermal oxidation film is included) and a nitride, in a semi-conductor substrate like a single crystal silicon substrate and the semi-conductor substrate front face, a light transmission nature substrate like a quartz substrate (Silica glass) or a glass substrate or a metal substrate, and an alumina, etc. are raised, for example. Such 2nd base is suitably chosen according to the application of a semi-conductor member.

[0047] in [lamination (bonding)] this invention, the 2nd above-mentioned base, lamination (nonvesicular semi-conductor layer is located inside -- as) **, and a multilayer-structure object are acquired for the 1st above-mentioned base. In this invention, the structure by which the nonvesicular semi-conductor layer which constitutes the 1st base was directly stuck on the 2nd base also includes the structure by which insulator layers, such as an oxide film formed in the thing of a rice cake theory and the front face of a nonvesicular semi-conductor layer and a nitride, or film other than this were stuck on the 2nd base with the multilayer-structure object with which a nonvesicular semi-conductor layer is located inside. That is, a nonvesicular semi-conductor layer calls the structure to which a nonvesicular semi-conductor layer is located inside a multilayer-structure object compared with a porosity silicon layer the multilayer-structure object located inside.

[0048] What the lamination side of the 1st base and the 2nd base is made flat for can perform concrete lamination by sticking both at a room temperature. In addition, since lamination reinforcement is increased, anode plate junction, pressurization heat treatment, etc. can also be performed.

[0049] In [field of multilayer-structure object] this invention, a multilayer-structure object is separated in an ion-implantation layer. An ion-implantation layer is the structure which a minute cavity (Micro-cavity) or minute air bubbles (bubble) produced, and is brittle compared with other fields of a multilayer-structure object. Therefore, it is effectively separable using the brittleness. There is it as the concrete approach of separation, others, for example, the method of lower-**(ing). [approach / of applying external force to an ion-implantation layer]

[0050] Since an ion-implantation layer is porosity-like, cubical expansion of the ion-implantation layer is carried out by oxidizing an ion-implantation layer from the circumference of a wafer using this layer carrying out accelerating oxidation, and there is an approach by that force.

[0051] The ion-implantation layer is usually covered with the nonvesicular layer also in the periphery section, and needs to make the periphery section or pedion express after lamination or before that. If this lamination base is oxidized, accelerating oxidation will begin from the periphery section of an ion-implantation layer with porous huge surface area. Si is SiO2. Since the volume expands 2.27 times when becoming, when porosity is 56% or less, cubical expansion also of the oxidation ion-implantation layer

will be carried out. Since extent becomes small as oxidation goes to the core of a wafer, the cubical expansion of the oxidation ion-implantation layer of the periphery section of a wafer becomes large. For this, the force is ******** so that it may be in the situation same with having driven the wedge into the ion-implantation layer from the end face of a wafer surely, internal pressure may be applied only to an ion-implantation layer and it may divide in an ion-implantation layer. And since oxidation progresses to homogeneity around a wafer, a lamination wafer will be equally removed from the perimeter of a wafer. A multilayer-structure object will be divided as a result.

[0052] If this approach excellent in the homogeneity of oxidation is used according to this invention, a wafer can be divided with sufficient control using one process of the usual Si-IC process.

[0053] Thermal stress can be generated and a multilayer-structure object can also be made to separate by the brittle ion-implantation porous layer by heating a multilayer-structure object.

[0054] Moreover, by using laser, without heating the whole multilayer-structure object, only a certain specific layer is made to absorb energy, and it can heat. By using the laser of the wavelength absorbed only in an ion-implantation porous layer or the layer near the ion-implantation porosity, partial heating can be performed and, thereby, it can dissociate.

[0055] Furthermore, an ion-implantation porous layer can be rapidly heated by passing a current an ion-implantation porous layer or near the ion-implantation porosity.

[0056] A multilayer-structure object may be separated using this.

[0057] After separating the multilayer-structure object which sticks the 1st base of [removal of a porous layer], and the 2nd base, and is acquired in an ion-implantation layer, the ion-implantation layer which remains to the separated base is alternatively removable using that the mechanical strength of this ion-implantation layer is low, and surface area being large. Approaches using an etching reagent besides the mechanical approach using grinding and polish as the alternative removal approach, such as chemical etching and ion etching (for example, reactive ion etching: Reactive Ion Etching), are employable.

[0058] When performing alternative etching, and when a nonvesicular thin film is a single crystal Si, at least one kind of the mixed liquor of alcohol and hydrogen peroxide solution which added either at least is used for the etching reagent of usual Si, fluoric acid, or fluoric acid at the mixed liquor of alcohol and hydrogen peroxide solution which added either at least, buffered fluoric acid, or buffered fluoric acid, and the etching removal of the ion-implantation layer can be carried out. When the nonvesicular semiconductor layer consists of compound semiconductors, the etching removal of the ion-implantation layer can be carried out using an etching reagent with the quick etch rate of Si to a compound semiconductor.

[0059] Hereafter, the gestalt of operation of this invention is explained using a drawing.

[0060]

[Embodiment of the Invention]

[Example 1 of embodiment] drawing 1 is the type section Fig. showing the process of the example 1 of an embodiment of this invention.

[0061] First, 1st Si single crystal substrate 11 is prepared, and at least one-layer nonvesicular layer 12 is formed on the main front face (drawing 1 (a)). Since the property of a SOI base that Si single crystal substrate 11 is done is decided in the nonvesicular layer 12, a resistance nonappointed wafer, a common playback wafer, etc. may be used. Furthermore, SiO2 13 can also be formed in the outermost superficial layer. In this case, the semantics that a lamination interface can be separated from a barrier layer may be used.

[0062] Next, the ion implantation of at least one sort of elements is carried out among rare gas, hydrogen, and nitrogen from the main front face of the 1st substrate (drawing 1 (b)). It collects ion notes ON and, as for 14, it is desirable to become near the interface of 1st Si single crystal substrate 11 and the nonvesicular layer 12 or the nonvesicular layer 12 interior.

[0063] Next, as shown in drawing 1 (c), the front face of the 2nd substrate 15 and the 1st substrate is stuck at a room temperature.

[0064] When a single crystal Si is deposited, it is desirable to stick, after forming Oxidation Si in the front face of a single crystal Si by approaches, such as thermal oxidation. Although drawing 1 has shown signs that the 2nd base and 1st base were stuck through the insulating layer 13, when the

nonvesicular thin film 12 is not Si, or when the 2nd substrate is not Si, there may not be an insulating layer 13.
[0065] It is also possible to stick by the three-sheet pile on both sides of insulating sheet metal on the occasion of lamination.
[0066] Next, it collects ion notes ON and a substrate is separated by 14 (drawing 1 (d)). As an approach of separating, it heats the approach to which the external pressure of pressurization, hauling, shear, a wedge, etc. is applied, the approach to which heat is applied, the approach of expanding Porosity Si from the circumference by oxidation, and applying internal pressure in Porosity Si, and in the shape of a pulse, and although thermal stress is applied or there is the approach of softening etc., it is not limited to this approach.
[0067] Subsequently, it removes alternatively using the approach which collected ion notes ON from the separated base, and mentioned 14 above.
[0068] The semi-conductor base material obtained by this invention is shown in drawing 1 (e). On the 2nd base 15, evenly, lamination of the nonvesicular thin film 12, for example, the single crystal Si thin film, is carried out to homogeneity, and it is formed throughout a wafer at a large area. If the 2nd base and 1st base are stuck through an insulating layer 13, the semi-conductor member obtained in this way can be suitably used, even if it sees from the point of electronic device production by which insulating separation was carried out.
[0069] Si single crystal substrate 11 collects residual ion notes ON, removes a layer 14, and when ruined so that it cannot permit surface surface smoothness, after it performs surface flattening, it can use it again as 1st Si single crystal substrate 11 or the 2nd following base 15.
[0070] In using as 1st Si single crystal substrate 11 again, by compensating with an epitaxial layer a part for the thickness reduced by detached core thickness and surface treatment, by wafer thickness reduction, it is lost that it becomes impossible to use it and it becomes reusable semipermanently.
[0071] [Example 2 of embodiment] drawing 2 is the type section Fig. showing the process of the example 2 of an embodiment of this invention. 1st Si single crystal substrate 21 is prepared, the ion implantation of at least one sort of elements is carried out among rare gas, hydrogen, and nitrogen from the main front face of the 1st substrate, the interior is covered ion notes ON, and 22 is formed (drawing 2 (a)). The surface dry area according [the direction which formed SiO2 23 in the outermost superficial layer] to an ion implantation can be prevented. After removing SiO2 23, at least one-layer nonvesicular layer 24 is formed on the main front face (drawing 2 (b)).
[0072] Subsequently, as shown in drawing 2 (c), the front face of the 2nd substrate 26 and the 1st substrate is stuck at a room temperature.
[0073] When a single crystal Si is deposited, it is desirable to stick, after forming Oxidation Si in the front face of a single crystal Si by approaches, such as thermal oxidation. Although drawing 1 has shown signs that the 2nd substrate and 1st substrate were stuck through the insulating layer 25, when the nonvesicular thin film 24 is not Si, or when the 2nd substrate is not Si, there may not be an insulating layer 25.
[0074] It is also possible to insert insulating sheet metal on the occasion of lamination, and to stick by the three-sheet pile.
[0075] Next, it collects ion notes ON and a substrate is separated by 22 (drawing 2 (d)).
[0076] Subsequently, it collects ion notes ON and 22 is removed alternatively.
[0077] The semi-conductor member obtained by this invention is shown in drawing 2 (e). On the 2nd base 26, evenly, lamination of the nonvesicular thin film 24, for example, the single crystal Si thin film, is carried out to homogeneity, and it is formed throughout a wafer at a large area. If the 2nd base and 1st base are stuck through an insulating layer 25, the semi-conductor member obtained in this way can be suitably used, even if it sees from the point of electronic device production by which insulating separation was carried out.
[0078] Si single crystal substrate 21 collects residual ion notes ON, removes a layer 22, and when ruined so that it cannot permit surface surface smoothness, after it performs surface flattening, it can use it again as 1st Si single crystal substrate 21 or the 2nd following base 26.

[0079] [Example 3 of embodiment] drawing 3 is a type section Fig. for explaining the process of the example 3 of an embodiment of this invention.
[0080] As shown in drawing 3 , the process shown in the above-mentioned examples 1 and 2 of an embodiment is processed to both sides of the 1st base by using the 2nd two bases, and two semiconductor substrates are produced to coincidence.
[0081] It sets to drawing 3 and, for a porous layer, and 33 and 36, a nonvesicular thin film, and 34 and 37 are [the 1st base, and 32 and 35 / 31] SiO2. A layer, and 38 and 39 are the 2nd base. Drawing 3 (a) After giving the process shown in the example 1 of an embodiment to both sides of the 1st substrate 31, it is drawing showing the condition of sticking the 2nd base 38 and 39 on the both sides, respectively. Drawing 3 (b) The condition of having dissociated by porous layers 32 and 35 is shown like the example 1 of an embodiment, and drawing 3 (c) is drawing showing the condition of having removed porous layers 32 and 35.
[0082] 1st Si single crystal substrate 31 collects residual ion notes ON, removes a layer, and when ruined so that it cannot permit surface surface smoothness, after it performs surface flattening, it can use it again as 1st Si single crystal substrate 31 or the 2nd following base 38 (or 39).
[0083] The support substrates 38 and 39 may not be the same. Moreover, the nonvesicular thin films 33 and 36 may not have same both sides. Moreover, there may not be insulating layers 34 and 37.
[0084] Hereafter, a concrete example is given and this invention is explained.
[0085] (Example 1) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.30 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0086]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : SiO2 of a front face after forming 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at a 0.30 micrometer/min pan It lets it pass and is H+. The 5x1016cm-2 ion implantation was carried out by 40keV(s).
[0087] This SiO2 Superposition, after making it contact, when the layer front face and the front face of Si substrate (the 2nd base) prepared independently were annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. The ion-implantation layer was divided into two sheets near the projection range of an ion implantation, when it dissociated, since it had become porosity-like. It was ruined. Selective etching of the front face by the side of the 2nd base was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0088] The etch rate to this etching reagent of a nonvesicular Si single crystal was very low, and the amount of etching (about dozens of A) was thickness reduction which can be disregarded practically.
[0089] Thereby, the single crystal Si layer which had the thickness of 0.2 micrometers on Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**6nm.
[0090] The base by which the single crystal Si layer was furthermore transferred was heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0091] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0092] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st base side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0093] When supplying as the 1st substrate again, it became reusable semipermanently by compensating a wafer thickness decrement with an epitaxial layer. That is, epitaxial thickness serves as a wafer thickness decrement instead of 0.30 micrometers 2nd after a repeat, and an ion-implantation layer is

formed in the interior of an epitaxial layer.
[0094] (Example 2) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.50 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0095]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It lets the epitaxial layer of a 0.30 micrometer/min front face pass, and is H+. The 6x1016cm-2 ion implantation was carried out by 50keV(s).
[0096] This epitaxial layer front face and 500nm SiO2 prepared independently Superposition, after making it contact, when the front face of Si substrate (the 2nd base) in which the layer was formed was annealed at 550 degrees C, it separated into two sheets near the projection range of an ion implantation. It was ruined. Selective etching of the front face by the side of the 2nd base was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0097] The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, and the amount of etching (about dozens of A) is thickness reduction which can be disregarded practically.
[0098] Then, flattening only of the pole front face was ground and carried out.
[0099] Thereby, the single crystal Si layer which had the thickness of 0.5 micrometers on Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 498nm**15nm.
[0100] When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0101] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0102] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0103] When supplying as the 1st substrate again, it became reusable semipermanently by compensating a wafer thickness decrement with an epitaxial layer. That is, epitaxial thickness serves as a wafer thickness decrement instead of 0.50 micrometers 2nd after a repeat, and an ion-implantation layer is formed in the interior of an epitaxial layer.
[0104] (Example 3) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.30 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0105]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.30 micrometer/min pan. Subsequently, SiO2 of a front face It lets a layer pass and is H+. 5x1016cm-2 ion was poured in by 40keV(s).
[0106] This SiO2 A layer front face and 500nm SiO2 prepared independently Superposition, after making it contact, when the front face of Si substrate (the 2nd base) in which the layer was formed was annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. Selective etching was carried out agitating the ion-implantation layer which remained in the 2nd substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0107] In this way, the single crystal Si layer which had the thickness of 0.2 micrometers on Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**6nm.
[0108] Subsequently, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force

microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0109] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0110] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st base side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0111] (Example 4) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.30 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0112]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.30 micrometer/min pan. SiO2 of a front face It lets a layer pass and is H+. 5x1016cm-2 ion was poured in by 40keV(s).
[0113] this SiO2 the superposition after carrying out plasma treatment of a layer front face and the front face of the fused-quartz substrate (the 2nd base) prepared independently and rinsing them -- it was made to contact When annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. Since the ion-implantation layer has become porosity-like, it is ruined. Selective etching of the front face by the side of the 2nd base was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0114] In this way, the single crystal Si layer which had the thickness of 0.2 micrometers on the transparent quartz substrate has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**6nm.
[0115] Next, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0116] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0117] Moreover, selective etching is carried out, also agitating after that the ion-implantation layer which remained in the 1st base side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 1st base again.
[0118] (Example 5) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.50 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0119]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.30 micrometer/min pan. Subsequently, SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 60keV(s).
[0120] this SiO2 the superposition after carrying out plasma treatment of a layer front face and the front face of the silicon on sapphire (the 2nd base) prepared independently and rinsing them -- it was made to contact When annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. Selective etching of the front face by the side of the 2nd substrate was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0121] Then, flattening only of the pole front face was carried out by polish.

[0122] In this way, the single crystal Si layer which had the thickness of 0.4 micrometers on transparent silicon on sapphire has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 402nm**12nm.
[0123] When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0124] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0125] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 1st base again.
[0126] (Example 6) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.60 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0127]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.30 micrometer/min pan. Next, SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 70keV(s).
[0128] this SiO2 the superposition after carrying out plasma treatment of a layer front face and the front face of the glass substrate (the 2nd substrate) prepared independently and rinsing them -- it was made to contact When annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. Selective etching of the front face by the side of the 2nd base was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0129] Then, flattening only of the pole front face was carried out by polish.
[0130] In this way, the single crystal Si layer which had the thickness of 0.5 micrometers on the transparent glass substrate has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 501nm**15nm.
[0131] When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0132] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0133] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 1st base again.
[0134] (Example 7) a 1st single crystal Si substrate top -- MOCVD (Metal Organic Chemical Vapor Deposition) -- 0.5 micrometers grew the single crystal GaAs epitaxially by law. The growth conditions are as follows.
[0135]
Source gas: TMG/AsH3 / H2 gas pressure : 80Torr temperature : It is 50nm SiO2 to this GaAs layer front face further 700 degrees C. The layer was formed. Subsequently, SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 60keV(s).
[0136] This SiO2 Superposition, after making it contact, when the layer front face and the front face of Si substrate (the 2nd base) prepared independently were annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. Since the ion-implantation layer had become

porosity-like, it was ruined. The front face by the side of the 2nd substrate was etched by 110 degrees C (ratio of 17ml : 3g : 8ml) of ethylenediamine + pyrocatechol + water.
[0137] The single crystal GaAs remained without being etched, as an ingredient of a dirty stop, selective etching of the remainder of an ion-implantation layer and 1st Si substrate was carried out, and the single crystal GaAs was removed completely.
[0138] In this way, the single crystal GaAs layer which had the thickness of 0.5 micrometers on Si substrate has been formed. When 100 points were measured for the thickness of the formed single crystal GaAs layer about the whole surface within a field, the homogeneity of thickness was 504nm**16nm.
[0139] When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to the GaAs wafer usually marketed by about 0.3nm.
[0140] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into a GaAs layer after the time of epitaxial growth, but it was checked that good crystallinity is maintained.
[0141] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st base side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again. (Example 8) a 1st single crystal Si substrate top -- MOCVD (Metal Organic Chemical Vapor Deposition) -- 0.7 micrometers grew the single crystal InP epitaxially by law.
[0142] Furthermore, it is 50nm SiO2 to this InP layer front face. The layer was formed. SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 80keV(s).
[0143] This SiO2 Superposition, after making it contact, when the layer front face and the front face of Si substrate (the 2nd substrate) prepared independently were annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. Since the ion-implantation layer has become porosity-like, it is ruined. Selective etching of the front face by the side of the 2nd substrate was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%.
[0144] The single crystal InP remained without being etched, as an ingredient of a dirty stop, selective etching of the remainder of an ion-implantation layer and 1st Si substrate was carried out, and the single crystal InP was removed completely.
[0145] In this way, the single crystal InP layer which had the thickness of 0.5 micrometers on Si substrate has been formed. When 100 points were measured for the thickness of the formed single crystal InP layer about the whole surface within a field, the homogeneity of thickness was 704nm**23nm.
[0146] When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to the InP wafer usually marketed by about 0.3nm.
[0147] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into an InP layer after the time of epitaxial growth, but it was checked that good crystallinity is maintained.
[0148] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st base side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0149] (Example 9) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.30 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0150]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.30 micrometer/min pan. Subsequently, SiO2 of a front face It lets a layer pass and is

helium+. The 5x1016cm-2 ion implantation was carried out by 80keV(s).
[0151] This SiO2 Superposition, after making it contact, when the layer front face and the front face of Si substrate (the 2nd substrate) prepared independently were annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. Selective etching of the front face by the side of the 2nd base is carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0152] In this way, the single crystal Si layer which had the thickness of 0.2 micrometers on Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**6nm.
[0153] Furthermore, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0154] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0155] Moreover, selective etching is carried out, also agitating after that the ion-implantation layer which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0156] (Example 10) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.30 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0157]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.30 micrometer/min pan. SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 40keV(s).
[0158] This SiO2 The layer front face and the front face of Si substrate (the 2nd substrate) prepared independently were piled up, and were contacted.
[0159] A 1st substrate side to CO2 after removing the rear-face oxide film of the 1st substrate Laser was irradiated all over the wafer. CO2 Laser is 200nm SiO2 of a lamination interface. It was absorbed by the layer, and the temperature of the near rose rapidly and was separated into two sheets near the projection range of an ion implantation by the rapid thermal stress in an ion-implantation layer. Continuation or a pulse is also available for laser.
[0160] Selective etching of the front face by the side of the 2nd base was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0161] In this way, the single crystal Si layer which had the thickness of 0.2 micrometers on Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**6nm.
[0162] Furthermore, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0163] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0164] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0165] (Example 11) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.30

micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0166]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.30 micrometer/min pan. Subsequently, SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 40keV(s).
[0167] This SiO2 They are a layer front face and the front face of Si substrate (the 2nd substrate) prepared independently SiO2 of the lamination wafer end face superposition and after making it contact When the layer and the epitaxial Si layer were exfoliated by etching, ion-implantation **** appeared.
[0168] When 1000-degree C PAIRO oxidation was carried out, two substrates separated the lamination wafer completely in the ion-implantation layer in 10 hours. When the field which exfoliated was observed, the ion-implantation layer of the wafer periphery section is SiO2. Although it was changing, the center section was still origin mostly.
[0169] Then, selective etching was carried out, agitating the ion-implantation layer which remained in the 2nd substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0170] In this way, the single crystal Si layer which had the thickness of 0.2 micrometers on Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**6nm.
[0171] Furthermore, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0172] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0173] Moreover, selective etching is carried out, also agitating after that the ion-implantation layer which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0174] (Example 12) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.30 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0175]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.30 micrometer/min pan. SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 40keV(s).
[0176] this SiO2 the superposition after carrying out plasma treatment of a layer front face and the front face of Si substrate (the 2nd base) prepared independently and rinsing them -- it was made to contact Heat treatment of 300 degrees C - 1 hour was performed, and lamination reinforcement was raised. When the wedge was put in from the perimeter of a lamination substrate, it separated into two sheets near the projection range of an ion implantation. Since the ion-implantation layer has become porosity-like, it is ruined. Selective etching of the front face by the side of the 2nd base is carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0177] That is, the single crystal Si layer which had the thickness of 0.2 micrometers on Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**6nm.
[0178] Furthermore, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.

[0179] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0180] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0181] (Example 13) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.30 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0182]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.30 micrometer/min pan. Next, SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 40keV(s).
[0183] this SiO2 the superposition after carrying out plasma treatment of a layer front face and the front face of Si substrate (the 2nd substrate) prepared independently and rinsing them -- it was made to contact Heat treatment of 300 degrees C - 1 hour was performed, and lamination reinforcement was raised. When shearing force was applied to the lamination substrate, it separated into two sheets near the projection range of an ion implantation. Selective etching of the front face by the side of the 2nd substrate was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0184] That is, the single crystal Si layer which had the thickness of 0.2 micrometers on Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**6nm.
[0185] Furthermore, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0186] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0187] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0188] When supplying as the 1st base again, it became reusable semipermanently by compensating a wafer thickness decrement with an epitaxial layer. That is, epitaxial thickness serves as a wafer thickness decrement instead of 0.30 micrometers 2nd after a repeat, and an ion-implantation layer is formed in the interior of an epitaxial layer.
[0189] (Example 14) It is H+ to the main front face on the 1st single crystal Si substrate. The 5x1016cm-2 ion implantation was carried out by 10keV(s). subsequently, CVD (Chemical Vapor Deposition) -- 0.30 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0190]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : In a 0.30 micrometer/min pan, it is 200nm SiO2 to this epitaxial Si layer front face. The layer was formed.
[0191] This SiO2 Superposition, after making it contact, when the layer front face and the front face of Si substrate (the 2nd substrate) prepared independently were annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. Since the ion-implantation layer has become porosity-like, it is ruined. Selective etching of the front face by the side of the 2nd substrate was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single

crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0192] Furthermore, the remainder of the 1st substrate equivalent to the ion-implantation depth was removed by etching.
[0193] In this way, the single crystal Si layer which had the thickness of 0.2 micrometers on Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**7nm.
[0194] Furthermore, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0195] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0196] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st base side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0197] (Example 15) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.50 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0198]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : At the time of 0.30 micrometer/min **, doping gas was added and it considered as n+Si/n-Si/Si substrate structure.
[0199] Furthermore, it formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation. Subsequently, SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 40keV(s).
[0200] This SiO2 Superposition, after making it contact, when the layer front face and the front face of Si substrate (the 2nd substrate) prepared independently were annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. Selective etching of the front face by the side of the 2nd substrate was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0201] In this way, n+ which had the thickness of 0.2 micrometers on Si oxide film The single crystal Si layer with an embedding layer has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**6nm.
[0202] Furthermore, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0203] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0204] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0205] (Example 16) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.30 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0206]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : At the time of 0.30 micrometer/min **, doping gas was added and it considered as n+Si/n-Si/Si substrate structure.

[0207] Furthermore, it is 50nm SiO2 by thermal oxidation to this epitaxial Si layer front face. The layer was formed. SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 40keV(s).
[0208] This SiO2 A layer front face and 500nm SiO2 prepared independently Superposition, after making it contact, when the front face of Si substrate (the 2nd base) in which the layer was formed was annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. Selective etching of the front face by the side of the 2nd base was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0209] In this way, n+ which had the thickness of 0.29 micrometers on Si oxide film The single crystal Si layer with an embedding layer has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 291nm**9nm.
[0210] Furthermore, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0211] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0212] Moreover, selective etching is carried out, also agitating after that the ion-implantation layer which remained in the 1st base side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0213] (Example 17) About the above-mentioned examples 1-16, the same processing as both sides of the 1st base was performed, and the semi-conductor member was obtained.
[0214]
[Effect of the Invention] As mentioned above, as explained, in the manufacture approach of the semi-conductor member of this invention, the 1st base for lamination bases is constituted using the nonvesicular semi-conductor layer allotted on the silicon substrate. A nonvesicular semi-conductor layer cannot be suitably constituted from an epitaxial semi-conductor layer, and a quality semi-conductor member can be offered from not being influenced in this case of a flow pattern defect peculiar to the above-mentioned silicon wafer, or COP (Crystal Originated Particles).
[0215] Moreover, since a nonvesicular semi-conductor layer can control an electric conduction mold and high impurity concentration easily, the manufacture approach of the semi-conductor member of this invention becomes what may satisfy various demands, and is high. [of application]
[0216] Furthermore, after separating the multilayer-structure object which sticks the 1st base and 2nd base and is acquired in an ion-implantation layer, since the silicon substrate which remained in the 1st base side is reusable as a configuration member of the 1st base or the 2nd base, it has an advantage also in respect of saving resources and low-cost-izing.
[0217] That is, the manufacture approach of a semi-conductor member of having excelled in the field of productivity, homogeneity, a controllability, and cost when obtaining the single crystal half conductor layer excellent in crystallinity on the 2nd base which can be constituted from an insulating substrate etc. according to this invention can be offered.

[Translation done.]

* NOTICES *

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the manufacture approach of a semi-conductor member including the process which transfers especially a semi-conductor layer on another base (transfer) about the manufacture approach of the semi-conductor member for forming semiconductor devices, such as a semiconductor integrated circuit, and a solar battery, semiconductor laser, light emitting diode.

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PRIOR ART

[Description of the Prior Art] The semi-conductor member shall be known under the name of the semi-conductor wafer, the semi-conductor substrate, the semiconductor device, etc., and shall contain that in which the semiconductor device is formed using the semiconductor region, and the thing of the condition before a semiconductor device is formed.
[0003] In such a semi-conductor member, some which have a semi-conductor layer are in an insulating lifter.
[0004] Formation of the single crystal Si semi-conductor layer of an insulating lifter is silicon. ON It was widely known as an insulator (SOI) technique, and in the bulk Si substrate which produces the usual Si integrated circuit, since the device using a SOI technique has many dominance points which cannot reach, many researches have accomplished. that is, 3. stray capacity which 1. dielectric separation is easy for, and is excellent in the possibility of high integration and 2. opposite radiation resistance using a SOI technique decreases -- having -- the possibility of improvement in the speed, and 4. -- a well -- the possibility of the perfect depletion mold field-effect transistor by the formation of 6. thin film which can prevent 5. latch rise which can skip a process, and the dominance point of ** are acquired. These are detailed in the following reference. SpecialIssue: "Single-crystal silicon on non-single-crystal insulators";edited by G.W.Cullen, Journal of Crystal Growth, volume 63 no 3 pp 429-590 (1983).
[0005] Furthermore in the past several years, many reports are made as a substrate with which SOI realizes improvement in the speed of MOSFET, and low-power-ization (IEEE SOI conference 1994). Moreover, since an insulating layer is in the lower part of a component when SOI structure is used, as a result of being able to simplify an isolation process compared with the case where a component is formed on a bulk Si wafer, a device process process is shortened. That is, together with high-performance-izing, low-pricing in total of wafer cost and process cost is expected compared with MOSFET on bulk Si, and IC.
[0006] Improvement in the speed according [the perfect depletion mold MOSFET] to improvement in driving force and low-power-ization are expected especially. Although the threshold voltage (Vth) of MOSFET is generally determined by the high impurity concentration of the channel section, in the case of the perfect depletion mold (FD;FullyDepleted) MOSFET using SOI, depletion-layer thickness will be influenced of the thickness of SOI. Therefore, in order to build a large-scale integrated circuit with the sufficient yield, homogeneity of SOI thickness was desired strongly.
[0007] Moreover, the device on a compound semiconductor has in Si the high engine performance which is not obtained, for example, a high speed, luminescence, etc. Most of these devices carries out epitaxial growth on compound semiconductor substrates, such as GaAs, and current is made in it. However, a compound semiconductor substrate is expensive, a mechanical strength is low, and a large area wafer has which trouble with difficult production.
[0008] From such a thing, it is cheap, and a mechanical strength is also high and the attempt which carries out heteroepitaxial growth of the compound semiconductor on Si wafer which can produce a large area wafer is made.
[0009] The research on formation of a SOI substrate was prosperous from around the 1970s. In early

stages, the approach (SOS:Sapphire on Silicon) of carrying out heteroepitaxial growth of the single crystal Si on the silicon on sapphire which is an insulating material, the approach (FIPOS:Fully Isolation by Porous Oxidized Silicon) of forming SOI structure according to the dielectric separation by oxidation of Porosity Si, and oxygen ion-implantation were often studied.

[0010] The FIPOS method is the approach of carrying out dielectric separation of the N type Si island by accelerating oxidation, after porosity-izing only a P type Si substrate by the anodization method in HF solution so that an N type Si layer may be formed in a P type Si single crystal substrate front face at island shape by the proton ion implantation, (J.Crystal Growth besides Imai, vol 63,547) (1983), or epitaxial growth and patterning and Si island may be surrounded from a front face. By this approach, Si field separated is determined before the device process, and there is a trouble that the degree of freedom of a device design may be restricted.

[0011] Oxidation ion-implantation is an approach called SIMOX reported for the first time by KIzumi. It is 1017-1018-/cm2 about oxygen ion to Si wafer. After carrying out extent impregnation, it anneals at the elevated temperature of about 1320 degrees in an argon and an oxygen ambient atmosphere. Consequently, the oxygen ion poured in focusing on the depth equivalent to the projection range (Rp) of an ion implantation combines with Si, and an oxidation Si layer is formed. In that case, Si layer made amorphous by the oxygen ion implantation of the upper part of an oxidation Si layer is also recrystallized, and it becomes a single crystal Si layer. the defect included in surface Si layer -- conventional 105 / cm2 although many -- the amount of placing of oxygen -- 4x1017-/cm2 carrying out near -- it is -102 / cm2 up to -- it has succeeded in decreasing. However, since the range of the impregnation energy which can maintain the crystallinity of the membraneous quality of an oxidation Si layer and a surface Si layer etc., and an injection rate was narrow, the thickness of a surface Si layer and an embedding oxidation Si layer (BOX;Burried Oxide) was restricted to the specific value. In order to obtain the surface Si layer of desired thickness, sacrifice oxidation or to grow epitaxially were required. In that case, as a result of being superimposed on the degraded minute by these processes, there is a trouble that thickness homogeneity deteriorates in distribution of thickness.

[0012] Moreover, it is reported that the poor formation field of Oxidation Si where SIMOX is called a pipe exists. As one of the cause of this, foreign matters, such as dust at the time of impregnation, are considered. In the part in which a pipe exists, degradation of a device property will arise by leak between a barrier layer and a support substrate.

[0013] As the above-mentioned [the ion implantation of SIMOX], since there are many injection rates compared with the ion implantation used in the usual semi-conductor process, even if the equipment of dedication is developed, in addition, impregnation time amount is long. Since an ion implantation carries out the raster scan of the ion beam of the predetermined amount of currents, or extends a beam and is performed, increase of impregnation time amount is assumed with large-area-izing of a wafer. Moreover, in elevated-temperature heat treatment of a large area wafer, it is pointed out that problems, such as generating of the slip by the temperature distribution in a wafer, become severeer. In SIMOX, in Si semi-conductor process of 1320 degrees C, since the elevated temperature which is not usually used needs to be heat-treated, we are anxious about the importance of this problem becoming still larger including equipment development.

[0014] Moreover, apart from the formation approach of the above conventional SOI, the approach of using heat treatment or adhesives for another Si single crystal substrate which oxidized Si single crystal substrate thermally, and forming lamination and SOI structure is capturing the spotlight in recent years. This approach needs to thin-film-ize the barrier layer for a device to homogeneity. That is, it is necessary to thin-film-ize Si single crystal substrate with a thickness of hundreds of micrometers less than [mum order or it]. There are three kinds of approaches in this thin film-ization as follows.

(1) It is difficult to thin-film-ize to homogeneity in the polish of thin-film-izing (1) by the thin film-ized (3). selective etching by thin film-ized (2). partial plasma etching by . polish. Especially as for thin film-ization of sub mum, dispersion also becomes dozens of% and this equalization poses a big problem. If diameter-ization of macrostomia of a wafer furthermore progresses, whenever [the / difficult] will just increase.

[0015] After thin-film-izing the approach of (2) by the approach by polish of (1) to about 1-3 micrometers by the approach of (1) beforehand, it carries out multipoint measurement of the thickness distribution on the whole surface. next -- this thickness distribution -- being based -- SF6 with a diameter of several mm etc. -- it etches amending thickness distribution by making the used plasma scan, and thin-film-izes to desired thickness. By this approach, it is reported that thickness distribution is made to about **10mm. However, since this foreign matter will serve as an etching mask if there is a substrate top foreign matter (particle) in the case of plasma etching, a projection will be formed on a substrate.
[0016] Moreover, since the front face is ruined immediately after etching, touch polishing is required after plasma-etching termination, but since control of the amount of polishing is performed by time management, control of the last thickness and degradation of the thickness distribution by polishing are pointed out. Since abrasive materials, such as colloidal silica, furthermore grind the front face which becomes a barrier layer directly against polish, we are anxious also about formation of the crushing layer by polish, and installation of processing distortion. Since plasma-etching time amount increases in proportion to increase of wafer area when a wafer is furthermore large-area-ized, we are anxious also about the remarkable fall of a throughput.
[0017] The approach of (3) is the approach of building the film configuration in which selective etching is possible to the substrate thin-film-ized beforehand. For example, it is 1019-/cm3 about boron on a P type substrate. The laminating of the thin layer of P+-Si and the thin layer of P type Si which were included in the above concentration is carried out by approaches, such as epitaxial growth, and it considers as the 1st substrate. After sticking this with the 2nd substrate through insulating layers, such as an oxide film, the rear face of the 1st substrate is beforehand made thin by grinding and polish. Then, it is P+ by the selective etching of a P type layer. It is a layer to exposure and a pan P+ A P type layer is exposed by the selective etching of a layer, and SOI structure is completed. This approach is detailed to the report of Maszara (W. P.Maszara, J.Electrochem.Soc., vol.138,341 (1991)).
[0018] although selective etching is effective in uniform thin-film-izing - at most 102 A selection ratio is not enough.
[0019] - Since the front-face nature after etching is bad, a touch polish is needed after etching. However, while thickness decreases as a result, thickness homogeneity also tends to deteriorate. Although especially polishing manages the amount of polishes by time amount, since dispersion in a polish rate is large, control of the amount of polishes is difficult. Therefore, in formation of an ultra-thin SOI layer, such as 100nm, it becomes especially a problem.
[0020] - Since the epitaxial growth or heteroepitaxial growth on an ion implantation and a high concentration B dope Si layer is used, the crystallinity of a SOI layer is bad. Moreover, the front-face nature of a lamination-ed side is also inferior to the usual Si wafer.
there is a trouble of ** (C. -- Harendt, et.al., and J.Elect.Mater.Vol.20,267 (1991) --) H. Baumgart, et.al.Extended Abstract of ECS 1st International Symposium of Wafer Bonding, pp-733 (1991), C. E.Hunt, Extended Abstract of ECS 1st International Symposium of Wafer Bonding, pp-696 (1991). Moreover, it depends for the selectivity of selective etching on the concentration difference and the steepness of the depth direction profile of impurities, such as boron, greatly. Therefore, if hot epitaxial growth is performed in order to raise hot bonding annealing for raising lamination reinforcement, and crystallinity, the depth direction distribution of high impurity concentration will spread, and the selectivity of etching will deteriorate. That is, coexistence of improvement in lamination reinforcement was difficult for the crystallinity of improvement in the selection ratio of etching.
[0021] Meanwhile, these people proposed the manufacture approach of a new semi-conductor member in JP,5-21338,A previously. The approach indicated by the official report concerned is a thing as follows. That is, after it forms the member which allotted the nonvesicular single crystal semiconductor region on a porosity single crystal semiconductor region and a front face sticks the front face of the member which consisted of insulating matter on the front face of said nonvesicular single crystal semiconductor region, it is the manufacture approach of the semi-conductor member characterized by removing said porosity single crystal semiconductor region by etching.

[0022] Moreover, Maibara and others which is the artificer of this invention was excellent in thickness homogeneity or crystallinity, and reported lamination SOI in which batch processing is possible (64 T. Yonehara et.al., Appl.Phys.Lett.vol. 2108 (1994)). Hereafter, the production approach of this lamination SOI is explained using drawing 4 (a) - (c).
[0023] By this approach, the porous layer 42 on the Si substrate 41 is used as an ingredient which performs selective etching. On a porous layer 42, the nonvesicular single crystal Si layer 43 is stuck with the 2nd substrate 44 through the oxidation Si layer 45, after growing epitaxially (drawing 4 (a)). Lamination of the 1st substrate is carried out by approaches, such as polish, from a rear face, and Porosity Si is exposed on the whole substrate surface (drawing 4 (b)). the exposed porosity Si -- KOH and HF+H 2O2 etc. -- it etches with a selection etching reagent and removes (drawing 4 (c)). Since the selection ratio of etching to the bulk Si of Porosity Si (nonvesicular single crystal Si) can be made high enough with 100,000 times at this time, the nonvesicular single crystal Si layer which grew on porosity beforehand can be transferred on the 2nd substrate, without reducing most thickness (transfer), and a SOI substrate can be formed. Therefore, the thickness homogeneity of SOI is mostly determined at the time of epitaxial growth. Since epitaxial growth can use the CVD system usually used in a semi-conductor process, as for the homogeneity, according to Sato's and others report (SSDM95), less than [100nm**2%] is realized. Moreover, the crystallinity of an epitaxial Si layer is also good and they are 3.5x102 / cm2. It was reported.
[0024] By the conventional approach, since the selectivity of etching was based on the difference and the profile of the depth direction of high impurity concentration, the temperature (lamination, epitaxial growth, oxidation, etc.) of heat treatment which extends concentration distribution was greatly restrained in general with 800 degrees C or less. On the other hand, since etching in this approach has determined the rate of etching of the difference of the structure of porosity and bulk, it is reported that constraint of heat treatment temperature is small and heat treatment of about 1180 degrees C is possible. For example, heat treatment after lamination raises the bond strength of wafers, and decreasing the number of the openings (void) produced in a lamination interface and magnitude is known. moreover, ** -- by etching based on a structure difference [like], even if there is particle which adhered on Porosity Si, thickness homogeneity is not affected.
[0025] However, the semi-conductor substrate using lamination surely needs two wafers, most is almost vainly removed by polish, etching, etc., one sheet is thrown away, and the resource of the limited earth is [among those] useless [a sheet]. Therefore, in SOI by lamination, the controllability, the homogeneous formation of other low cost, and improvement in economical efficiency are just going to desire.
[0026] That is, coincidence was expected saving resources by the reuse of a wafer etc., and the method of realizing a cost cut while quality produced enough SOI substrates with sufficient repeatability.
[0027] Meanwhile, after these people stuck two substrates previously, they separated the stuck substrate in the porous layer, removed residual porosity from one substrate after separation, and proposed the manufacture approach of the semi-conductor substrate which reuses this substrate by JP,7-302889,A. Drawing 5 (a) - (c) is used for below, and one example of the approach indicated by the official report concerned is explained to it.
[0028] After porosity-izing the surface layer of the 1st Si substrate 51 and forming a porous layer 52, the single crystal Si layer 53 is formed on it, and the principal plane of 2nd Si substrate 54 with another this single crystal Si layer and 1st Si base is stuck through an insulating layer 55 (drawing 5 (a)). Then, a SOI substrate is formed by dividing the wafer stuck by the porous layer (drawing 5 (b)), and removing alternatively the porosity Si layer exposed to the front face by the side of 2nd Si base (drawing 5 (c)). The 1st substrate 41 can remove and reuse the porous layer which remained.
[0029] Invention indicated by JP,7-302889,A is very useful when attaining low cost-ization of a semi-conductor substrate, since the substrate with which the structure of a porosity silicon layer dissociates and used the substrate for the making process of a semi-conductor substrate once using the brittle point compared with nonvesicular silicon can be again used for the making process of a semi-conductor substrate.

[0030] Independently, after forming the semi-conductor layer which constitutes the photo-electric-conversion section of a solar battery on a porosity silicon layer, separating this semi-conductor layer from a porous layer is indicated by JP,8-213645,A, and it is too indicated to be this to it to reuse the substrate with which the porosity silicon layer was formed also here.
[0031] On the other hand, although a base is separated using such a porosity silicon layer, otherwise, the technique of separating a base, without using such a porosity silicon layer is indicated by JP,5-211128,A. The approach of making a bubble layer by the ion implantation in a silicon substrate, making this bubble layer producing the crystal rearrangement by heat treatment and condensation of air bubbles, and removing the field by the side of the outermost surface of a silicon substrate (called "the thin semiconductor material film" in this official report) bordering on a bubble layer is indicated by this official report. In short, the impregnation ion of the bulk Si outermost surface does not exist, or a thin semiconductor material film here is a field with very little abundance. However, in Si wafer of bulk, they are a flow pattern defect (FPD;Flow Pattern Defect) (T. Abe, Extended Abst.Electrochem.Soc.Spring Meeting vol.95-1, pp.596, (May, 1995)) and COP (Crystal Originated Particles) (Hidekazu Yamamoto).

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] As mentioned above, as explained, in the manufacture approach of the semi-conductor member of this invention, the 1st base for lamination bases is constituted using the nonvesicular semi-conductor layer allotted on the silicon substrate. A nonvesicular semi-conductor layer cannot be suitably constituted from an epitaxial semi-conductor layer, and a quality semi-conductor member can be offered from not being influenced in this case of a flow pattern defect peculiar to the above-mentioned silicon wafer, or COP (Crystal Originated Particles).
[0215] Moreover, since a nonvesicular semi-conductor layer can control an electric conduction mold and high impurity concentration easily, the manufacture approach of the semi-conductor member of this invention becomes what may satisfy various demands, and is high. [of application]
[0216] Furthermore, after separating the multilayer-structure object which sticks the 1st base and 2nd base and is acquired in an ion-implantation layer, since the silicon substrate which remained in the 1st base side is reusable as a configuration member of the 1st base or the 2nd base, it has an advantage also in respect of saving resources and low-cost-izing.
[0217] That is, the manufacture approach of a semi-conductor member of having excelled in the field of productivity, homogeneity, a controllability, and cost when obtaining the single crystal half conductor layer excellent in crystallinity on the 2nd base which can be constituted from an insulating substrate etc. according to this invention can be offered.

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TECHNICAL PROBLEM

It is becoming clear that defects peculiar to it, such as a "demand technical problem to diameter silicon wafer of macrostomia" 23rd ultra Clean Technology college and (Aug.1996), exist. Therefore, a flow pattern defect and COP will exist in this thin semiconductor material film.

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MEANS

[Means for Solving the Problem] The process which prepares the 1st base which has the ion-implantation layer of the nonvesicular semi-conductor layer matched with the means of this invention on the silicon substrate and this silicon substrate, said silicon substrate, or said nonvesicular semi-conductor layer formed in either at least, The process which sticks said the 1st base and 2nd base so that the multilayer-structure object with which said nonvesicular semi-conductor layer is located inside may be acquired, It is in offering the manufacture approach of the semi-conductor member characterized by having the process which separates said multilayer-structure object in said ion-implantation layer, and the process which removes the ion-implantation layer which remained in said separated 2nd base side.
[0035] The process which prepares the 1st base which has the ion-implantation layer of the nonvesicular semi-conductor layer matched with still more nearly another means of this invention on the silicon substrate and this silicon substrate, said silicon substrate, or said nonvesicular semi-conductor layer formed in either at least, The process which sticks said the 1st base and 2nd base so that the multilayer-structure object with which said nonvesicular semi-conductor layer is located inside may be acquired, The process which separates said multilayer-structure object in said ion-implantation layer, the process which removes the ion-implantation layer which remained in said separated 2nd base side, It is in the thing of the semi-conductor member characterized by having the process which uses the base which removes the ion-implantation layer which remained in said separated 1st base side, and is obtained as a raw material of said 1st base for which the manufacture approach offer is made.
[0036] The process which prepares the 1st base which has the ion-implantation layer of the nonvesicular semi-conductor layer matched with still more nearly another means of this invention on the silicon substrate and this silicon substrate, said silicon substrate, or said nonvesicular semi-conductor layer formed in either at least, The process which sticks said the 1st base and 2nd base so that the multilayer-structure object with which said nonvesicular semi-conductor layer is located inside may be acquired, The process which separates said multilayer-structure object in said ion-implantation layer, the process which removes the ion-implantation layer which remained in said separated 2nd base side, It is in offering the manufacture approach of the semi-conductor member characterized by having the process which uses the base which removes the ion-implantation layer which remained in said separated 1st base side, and is obtained as a raw material of said 2nd base.

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OPERATION

In the manufacture approach of the semi-conductor member of [operation] this invention, the 1st base for lamination bases is constituted using the nonvesicular semi-conductor layer allotted on the silicon substrate. A nonvesicular semi-conductor layer cannot be suitably constituted from an epitaxial semi-conductor layer, and a quality semi-conductor member can be offered from not being influenced in this case of a flow pattern defect peculiar to the above-mentioned silicon wafer, or COP (Crystal Originated Particles).
[0038] Moreover, since a nonvesicular semi-conductor layer can control an electric conduction mold and high impurity concentration easily, the manufacture approach of the semi-conductor member of this invention becomes what may satisfy various demands, and is high. [of application]
[0039] Furthermore, after separating the multilayer-structure object which sticks the 1st base and 2nd base and is acquired in an ion-implantation layer, since the silicon substrate which remained in the 1st base side is reusable as a configuration member of the 1st base or the 2nd base, it has an advantage also in respect of saving resources and low-cost-izing.
[0040] The manufacture approach of a semi-conductor member of having excelled in the field of productivity, homogeneity, a controllability, and cost when obtaining the single crystal half conductor layer excellent in crystallinity on the 2nd base which can be constituted from an insulating substrate etc. according to this invention can be offered.
[0041]
[Embodiment of the Invention] Although the suitable example of an embodiment of this invention is described hereafter, this invention is not limited to these examples of an embodiment, and the purpose of this invention should just be attained.
[0042] When the ion implantation of helium or the hydrogen is carried out to a [ion-implantation layer] single crystal silicon substrate, a minute cavity (micro-cavity) with a diameter of several nm - dozens of nm is -1016 - 1017-/cm2 to the field by which the ion implantation was carried out. Being able to form by the thing consistency, this silicon substrate serves as structure which formed the porous layer in the interior. Usable ion consists of an element chosen from rare gas, hydrogen, and nitrogen in this invention. In this invention, even if there are few nonvesicular semi-conductor layers allotted on the silicon substrate or this silicon substrate, that what is necessary is to just be formed in either, an ion-implantation layer can also be formed in both interface, and can also be formed more than two-layer. The ion injection rate of the ion-implantation layer formed by this invention is 1016-1017-/cm2, when separation of the multilayer-structure object which sticks the 1st base and 2nd base and is acquired is taken into consideration. The range is desirable. Although the thickness of an ion-implantation layer changes with acceleration voltage, when taking into consideration making into homogeneity thickness of the nonvesicular semi-conductor layer on the 2nd base obtained by generally separating 500A or less and a multilayer-structure object, it is good to consider as 200A or less preferably. The ion-implantation layer has concentration distribution in the direction of thickness, and there is an inclination for concentration distribution of an ion injection rate to be separated in respect of being the highest, in the case of separation of a multilayer-structure object.

[0043] In [nonvesicular semi-conductor layer] this invention, compound semiconductors, such as GaAs besides a single crystal Si, Polycrystal Si, and amorphous Si, InP, GaAsP, GaAlAs, InAs, AlGaSb, InGaAs, ZnS, CdSe, CdTe, and SiGe, etc. can be suitably used as a nonvesicular semi-conductor layer. And a nonvesicular semi-conductor layer may already make semiconductor devices, such as FET (Field Efect Transistor).
[0044] In [1st base] this invention, the 1st base means the base which has the ion-implantation layer of a silicon substrate, the nonvesicular semi-conductor layer allotted on this silicon substrate, and a silicon substrate or a nonvesicular semi-conductor layer formed in either at least. Therefore, the substrate with which the 1st base formed the nonvesicular semi-conductor layer on the silicon substrate by which the ion-implantation layer was formed in the interior The thing of a rice cake theory, the thing in which insulator layers, such as a nitride and an oxide film, were formed on this nonvesicular semi-conductor layer, Or after forming an epitaxial semi-conductor layer and an insulating layer on a silicon substrate, the substrate which carried out the ion implantation to the silicon substrate, and formed the ion-implantation layer, the thing which formed the ion-implantation layer further into the nonvesicular semi-conductor layer formed on the silicon substrate are included.
[0045] In order to form a nonvesicular semi-conductor layer on a silicon substrate, a sputtering technique (a bias sputtering technique is included) besides CVD methods, such as reduced pressure CVD, plasma CVD, Light CVD, and MOCVD (Metal-Organic CVD), molecular beam epitaxy, a liquid phase grown method, etc. are employable.
[0046] As the 2nd base by which the [2nd base] nonvesicular semi-conductor layer is transferred (transfer), insulating substrates, such as what prepared insulator layers, such as an oxide film (the thermal oxidation film is included) and a nitride, in a semi-conductor substrate like a single crystal silicon substrate and the semi-conductor substrate front face, a light transmission nature substrate like a quartz substrate (Silica glass) or a glass substrate or a metal substrate, and an alumina, etc. are raised, for example. Such 2nd base is suitably chosen according to the application of a semi-conductor member.
[0047] in [lamination (bonding)] this invention, the 2nd above-mentioned base, lamination (nonvesicular semi-conductor layer is located inside -- as) **, and a multilayer-structure object are acquired for the 1st above-mentioned base. In this invention, the structure by which the nonvesicular semi-conductor layer which constitutes the 1st base was directly stuck on the 2nd base also includes the structure by which insulator layers, such as an oxide film formed in the thing of a rice cake theory and the front face of a nonvesicular semi-conductor layer and a nitride, or film other than this were stuck on the 2nd base with the multilayer-structure object with which a nonvesicular semi-conductor layer is located inside. That is, a nonvesicular semi-conductor layer calls the structure to which a nonvesicular semi-conductor layer is located inside a multilayer-structure object compared with a porosity silicon layer the multilayer-structure object located inside.
[0048] What the lamination side of the 1st base and the 2nd base is made flat for can perform concrete lamination by sticking both at a room temperature. In addition, since lamination reinforcement is increased, anode plate junction, pressurization heat treatment, etc. can also be performed.
[0049] In [field of multilayer-structure object] this invention, a multilayer-structure object is separated in an ion-implantation layer. An ion-implantation layer is the structure which a minute cavity (Micro-cavity) or minute air bubbles (bubble) produced, and is brittle compared with other fields of a multilayer-structure object. Therefore, it is effectively separable using the brittleness. There is it as the concrete approach of separation, others, for example, the method of lower-**(ing). [approach / of applying external force to an ion-implantation layer]
[0050] Since an ion-implantation layer is porosity-like, cubical expansion of the ion-implantation layer is carried out by oxidizing an ion-implantation layer from the circumference of a wafer using this layer carrying out accelerating oxidation, and there is an approach by that force.
[0051] The ion-implantation layer is usually covered with the nonvesicular layer also in the periphery section, and needs to make the periphery section or pedion express after lamination or before that. If this lamination base is oxidized, accelerating oxidation will begin from the periphery section of an ion-implantation layer with porous huge surface area. Si is SiO2. Since the volume expands 2.27 times when

becoming, when porosity is 56% or less, cubical expansion also of the oxidation ion-implantation layer will be carried out. Since extent becomes small as oxidation goes to the core of a wafer, the cubical expansion of the oxidation ion-implantation layer of the periphery section of a wafer becomes large. For this, the force is ******** so that it may be in the situation same with having driven the wedge into the ion-implantation layer from the end face of a wafer surely, internal pressure may be applied only to an ion-implantation layer and it may divide in an ion-implantation layer. And since oxidation progresses to homogeneity around a wafer, a lamination wafer will be equally removed from the perimeter of a wafer. A multilayer-structure object will be divided as a result.

[0052] If this approach excellent in the homogeneity of oxidation is used according to this invention, a wafer can be divided with sufficient control using one process of the usual Si-IC process.

[0053] Thermal stress can be generated and a multilayer-structure object can also be made to separate by the brittle ion-implantation porous layer by heating a multilayer-structure object.

[0054] Moreover, by using laser, without heating the whole multilayer-structure object, only a certain specific layer is made to absorb energy, and it can heat. By using the laser of the wavelength absorbed only in an ion-implantation porous layer or the layer near the ion-implantation porosity, partial heating can be performed and, thereby, it can dissociate.

[0055] Furthermore, an ion-implantation porous layer can be rapidly heated by passing a current an ion-implantation porous layer or near the ion-implantation porosity.

[0056] A multilayer-structure object may be separated using this.

[0057] After separating the multilayer-structure object which sticks the 1st base of [removal of a porous layer], and the 2nd base, and is acquired in an ion-implantation layer, the ion-implantation layer which remains to the separated base is alternatively removable using that the mechanical strength of this ion-implantation layer is low, and surface area being large. Approaches using an etching reagent besides the mechanical approach using grinding and polish as the alternative removal approach, such as chemical etching and ion etching (for example, reactive ion etching: Reactive Ion Etching), are employable.

[0058] When performing alternative etching, and when a nonvesicular thin film is a single crystal Si, at least one kind of the mixed liquor of alcohol and hydrogen peroxide solution which added either at least is used for the etching reagent of usual Si, fluoric acid, or fluoric acid at the mixed liquor of alcohol and hydrogen peroxide solution which added either at least, buffered fluoric acid, or buffered fluoric acid, and the etching removal of the ion-implantation layer can be carried out. When the nonvesicular semiconductor layer consists of compound semiconductors, the etching removal of the ion-implantation layer can be carried out using an etching reagent with the quick etch rate of Si to a compound semiconductor.

[0059] Hereafter, the gestalt of operation of this invention is explained using a drawing.

[0060]

[Embodiment of the Invention]

[Example 1 of embodiment] drawing 1 is the type section Fig. showing the process of the example 1 of an embodiment of this invention.

[0061] First, 1st Si single crystal substrate 11 is prepared, and at least one-layer nonvesicular layer 12 is formed on the main front face (drawing 1 (a)). Since the property of a SOI base that Si single crystal substrate 11 is done is decided in the nonvesicular layer 12, a resistance nonappointed wafer, a common playback wafer, etc. may be used. Furthermore, SiO2 13 can also be formed in the outermost superficial layer. In this case, the semantics that a lamination interface can be separated from a barrier layer may be used.

[0062] Next, the ion implantation of at least one sort of elements is carried out among rare gas, hydrogen, and nitrogen from the main front face of the 1st substrate (drawing 1 (b)). It collects ion notes ON and, as for 14, it is desirable to become near the interface of 1st Si single crystal substrate 11 and the nonvesicular layer 12 or the nonvesicular layer 12 interior.

[0063] Next, as shown in drawing 1 (c), the front face of the 2nd substrate 15 and the 1st substrate is stuck at a room temperature.

[0064] When a single crystal Si is deposited, it is desirable to stick, after forming Oxidation Si in the front face of a single crystal Si by approaches, such as thermal oxidation. Although drawing 1 has

shown signs that the 2nd base and 1st base were stuck through the insulating layer 13, when the nonvesicular thin film 12 is not Si, or when the 2nd substrate is not Si, there may not be an insulating layer 13.
[0065] It is also possible to stick by the three-sheet pile on both sides of insulating sheet metal on the occasion of lamination.
[0066] Next, it collects ion notes ON and a substrate is separated by 14 (drawing 1 (d)). As an approach of separating, it heats the approach to which the external pressure of pressurization, hauling, shear, a wedge, etc. is applied, the approach to which heat is applied, the approach of expanding Porosity Si from the circumference by oxidation, and applying internal pressure in Porosity Si, and in the shape of a pulse, and although thermal stress is applied or there is the approach of softening etc., it is not limited to this approach.
[0067] Subsequently, it removes alternatively using the approach which collected ion notes ON from the separated base, and mentioned 14 above.
[0068] The semi-conductor base material obtained by this invention is shown in drawing 1 (e). On the 2nd base 15, evenly, lamination of the nonvesicular thin film 12, for example, the single crystal Si thin film, is carried out to homogeneity, and it is formed throughout a wafer at a large area. If the 2nd base and 1st base are stuck through an insulating layer 13, the semi-conductor member obtained in this way can be suitably used, even if it sees from the point of electronic device production by which insulating separation was carried out.
[0069] Si single crystal substrate 11 collects residual ion notes ON, removes a layer 14, and when ruined so that it cannot permit surface surface smoothness, after it performs surface flattening, it can use it again as 1st Si single crystal substrate 11 or the 2nd following base 15.
[0070] In using as 1st Si single crystal substrate 11 again, by compensating with an epitaxial layer a part for the thickness reduced by detached core thickness and surface treatment, by wafer thickness reduction, it is lost that it becomes impossible to use it and it becomes reusable semipermanently.
[0071] [Example 2 of embodiment] drawing 2 is the type section Fig. showing the process of the example 2 of an embodiment of this invention. 1st Si single crystal substrate 21 is prepared, the ion implantation of at least one sort of elements is carried out among rare gas, hydrogen, and nitrogen from the main front face of the 1st substrate, the interior is covered ion notes ON, and 22 is formed (drawing 2 (a)). The surface dry area according [the direction which formed SiO2 23 in the outermost superficial layer] to an ion implantation can be prevented. After removing SiO2 23, at least one-layer nonvesicular layer 24 is formed on the main front face (drawing 2 (b)).
[0072] Subsequently, as shown in drawing 2 (c), the front face of the 2nd substrate 26 and the 1st substrate is stuck at a room temperature.
[0073] When a single crystal Si is deposited, it is desirable to stick, after forming Oxidation Si in the front face of a single crystal Si by approaches, such as thermal oxidation. Although drawing 1 has shown signs that the 2nd substrate and 1st substrate were stuck through the insulating layer 25, when the nonvesicular thin film 24 is not Si, or when the 2nd substrate is not Si, there may not be an insulating layer 25.
[0074] It is also possible to insert insulating sheet metal on the occasion of lamination, and to stick by the three-sheet pile.
[0075] Next, it collects ion notes ON and a substrate is separated by 22 (drawing 2 (d)).
[0076] Subsequently, it collects ion notes ON and 22 is removed alternatively.
[0077] The semi-conductor member obtained by this invention is shown in drawing 2 (e). On the 2nd base 26, evenly, lamination of the nonvesicular thin film 24, for example, the single crystal Si thin film, is carried out to homogeneity, and it is formed throughout a wafer at a large area. If the 2nd base and 1st base are stuck through an insulating layer 25, the semi-conductor member obtained in this way can be suitably used, even if it sees from the point of electronic device production by which insulating separation was carried out.
[0078] Si single crystal substrate 21 collects residual ion notes ON, removes a layer 22, and when ruined so that it cannot permit surface surface smoothness, after it performs surface flattening, it can use it

again as 1st Si single crystal substrate 21 or the 2nd following base 26.
[0079] [Example 3 of embodiment] drawing 3 is a type section Fig. for explaining the process of the example 3 of an embodiment of this invention.
[0080] As shown in drawing 3 , the process shown in the above-mentioned examples 1 and 2 of an embodiment is processed to both sides of the 1st base by using the 2nd two bases, and two semiconductor substrates are produced to coincidence.
[0081] It sets to drawing 3 and, for a porous layer, and 33 and 36, a nonvesicular thin film, and 34 and 37 are [the 1st base, and 32 and 35 / 31] SiO2. A layer, and 38 and 39 are the 2nd base. Drawing 3 (a) After giving the process shown in the example 1 of an embodiment to both sides of the 1st substrate 31, it is drawing showing the condition of sticking the 2nd base 38 and 39 on the both sides, respectively. Drawing 3 (b) The condition of having dissociated by porous layers 32 and 35 is shown like the example 1 of an embodiment, and drawing 3 (c) is drawing showing the condition of having removed porous layers 32 and 35.
[0082] 1st Si single crystal substrate 31 collects residual ion notes ON, removes a layer, and when ruined so that it cannot permit surface surface smoothness, after it performs surface flattening, it can use it again as 1st Si single crystal substrate 31 or the 2nd following base 38 (or 39).
[0083] The support substrates 38 and 39 may not be the same. Moreover, the nonvesicular thin films 33 and 36 may not have same both sides. Moreover, there may not be insulating layers 34 and 37.
[0084] Hereafter, a concrete example is given and this invention is explained.
[0085] (Example 1) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.30 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0086]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : SiO2 of a front face after forming 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at a 0.30 micrometer/min pan It lets it pass and is H+. The 5x1016cm-2 ion implantation was carried out by 40keV(s).
[0087] This SiO2 Superposition, after making it contact, when the layer front face and the front face of Si substrate (the 2nd base) prepared independently were annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. The ion-implantation layer was divided into two sheets near the projection range of an ion implantation, when it dissociated, since it had become porosity-like. It was ruined. Selective etching of the front face by the side of the 2nd base was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0088] The etch rate to this etching reagent of a nonvesicular Si single crystal was very low, and the amount of etching (about dozens of A) was thickness reduction which can be disregarded practically.
[0089] Thereby, the single crystal Si layer which had the thickness of 0.2 micrometers on Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**6nm.
[0090] The base by which the single crystal Si layer was furthermore transferred was heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0091] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0092] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st base side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0093] When supplying as the 1st substrate again, it became reusable semipermanently by compensating a wafer thickness decrement with an epitaxial layer. That is, epitaxial thickness serves as a wafer

thickness decrement instead of 0.30 micrometers 2nd after a repeat, and an ion-implantation layer is formed in the interior of an epitaxial layer.
[0094] (Example 2) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.50 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0095]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It lets the epitaxial layer of a 0.30 micrometer/min front face pass, and is H+. The 6x1016cm-2 ion implantation was carried out by 50keV(s).
[0096] This epitaxial layer front face and 500nm SiO2 prepared independently Superposition, after making it contact, when the front face of Si substrate (the 2nd base) in which the layer was formed was annealed at 550 degrees C, it separated into two sheets near the projection range of an ion implantation. It was ruined. Selective etching of the front face by the side of the 2nd base was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0097] The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, and the amount of etching (about dozens of A) is thickness reduction which can be disregarded practically.
[0098] Then, flattening only of the pole front face was ground and carried out.
[0099] Thereby, the single crystal Si layer which had the thickness of 0.5 micrometers on Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 498nm**15nm.
[0100] When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0101] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0102] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0103] When supplying as the 1st substrate again, it became reusable semipermanently by compensating a wafer thickness decrement with an epitaxial layer. That is, epitaxial thickness serves as a wafer thickness decrement instead of 0.50 micrometers 2nd after a repeat, and an ion-implantation layer is formed in the interior of an epitaxial layer.
[0104] (Example 3) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.30 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0105]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.30 micrometer/min pan. Subsequently, SiO2 of a front face It lets a layer pass and is H+. 5x1016cm-2 ion was poured in by 40keV(s).
[0106] This SiO2 A layer front face and 500nm SiO2 prepared independently Superposition, after making it contact, when the front face of Si substrate (the 2nd base) in which the layer was formed was annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. Selective etching was carried out agitating the ion-implantation layer which remained in the 2nd substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0107] In this way, the single crystal Si layer which had the thickness of 0.2 micrometers on Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**6nm.

[0108] Subsequently, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0109] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0110] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st base side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0111] (Example 4) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.30 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0112]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.30 micrometer/min pan. SiO2 of a front face It lets a layer pass and is H+. 5x1016cm-2 ion was poured in by 40keV(s).
[0113] this SiO2 the superposition after carrying out plasma treatment of a layer front face and the front face of the fused-quartz substrate (the 2nd base) prepared independently and rinsing them -- it was made to contact When annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. Since the ion-implantation layer has become porosity-like, it is ruined. Selective etching of the front face by the side of the 2nd base was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0114] In this way, the single crystal Si layer which had the thickness of 0.2 micrometers on the transparent quartz substrate has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**6nm.
[0115] Next, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0116] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0117] Moreover, selective etching is carried out, also agitating after that the ion-implantation layer which remained in the 1st base side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 1st base again.
[0118] (Example 5) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.50 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0119]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.30 micrometer/min pan. Subsequently, SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 60keV(s).
[0120] this SiO2 the superposition after carrying out plasma treatment of a layer front face and the front face of the silicon on sapphire (the 2nd base) prepared independently and rinsing them -- it was made to contact When annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. Selective etching of the front face by the side of the 2nd substrate was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.

[0121] Then, flattening only of the pole front face was carried out by polish.
[0122] In this way, the single crystal Si layer which had the thickness of 0.4 micrometers on transparent silicon on sapphire has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 402nm**12nm.
[0123] When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0124] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0125] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 1st base again.
[0126] (Example 6) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.60 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0127]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.30 micrometer/min pan. Next, SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 70keV(s).
[0128] this SiO2 the superposition after carrying out plasma treatment of a layer front face and the front face of the glass substrate (the 2nd substrate) prepared independently and rinsing them -- it was made to contact When annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. Selective etching of the front face by the side of the 2nd base was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0129] Then, flattening only of the pole front face was carried out by polish.
[0130] In this way, the single crystal Si layer which had the thickness of 0.5 micrometers on the transparent glass substrate has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 501nm**15nm.
[0131] When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0132] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0133] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 1st base again.
[0134] (Example 7) a 1st single crystal Si substrate top -- MOCVD (Metal Organic Chemical Vapor Deposition) -- 0.5 micrometers grew the single crystal GaAs epitaxially by law. The growth conditions are as follows.
[0135]
Source gas: TMG/AsH3 / H2 gas pressure : 80Torr temperature : It is 50nm SiO2 to this GaAs layer front face further 700 degrees C. The layer was formed. Subsequently, SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 60keV(s).
[0136] This SiO2 Superposition, after making it contact, when the layer front face and the front face of Si substrate (the 2nd base) prepared independently were annealed at 600 degrees C, it separated into two

sheets near the projection range of an ion implantation. Since the ion-implantation layer had become porosity-like, it was ruined. The front face by the side of the 2nd substrate was etched by 110 degrees C (ratio of 17ml : 3g : 8ml) of ethylenediamine + pyrocatechol + water.
[0137] The single crystal GaAs remained without being etched, as an ingredient of a dirty stop, selective etching of the remainder of an ion-implantation layer and 1st Si substrate was carried out, and the single crystal GaAs was removed completely.
[0138] In this way, the single crystal GaAs layer which had the thickness of 0.5 micrometers on Si substrate has been formed. When 100 points were measured for the thickness of the formed single crystal GaAs layer about the whole surface within a field, the homogeneity of thickness was 504nm**16nm.
[0139] When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to the GaAs wafer usually marketed by about 0.3nm.
[0140] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into a GaAs layer after the time of epitaxial growth, but it was checked that good crystallinity is maintained.
[0141] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st base side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again. (Example 8) a 1st single crystal Si substrate top -- MOCVD (Metal Organic Chemical Vapor Deposition) -- 0.7 micrometers grew the single crystal InP epitaxially by law.
[0142] Furthermore, it is 50nm SiO2 to this InP layer front face. The layer was formed. SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 80keV(s).
[0143] This SiO2 Superposition, after making it contact, when the layer front face and the front face of Si substrate (the 2nd substrate) prepared independently were annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. Since the ion-implantation layer has become porosity-like, it is ruined. Selective etching of the front face by the side of the 2nd substrate was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%.
[0144] The single crystal InP remained without being etched, as an ingredient of a dirty stop, selective etching of the remainder of an ion-implantation layer and 1st Si substrate was carried out, and the single crystal InP was removed completely.
[0145] In this way, the single crystal InP layer which had the thickness of 0.5 micrometers on Si substrate has been formed. When 100 points were measured for the thickness of the formed single crystal InP layer about the whole surface within a field, the homogeneity of thickness was 704nm**23nm.
[0146] When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to the InP wafer usually marketed by about 0.3nm.
[0147] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into an InP layer after the time of epitaxial growth, but it was checked that good crystallinity is maintained.
[0148] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st base side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0149] (Example 9) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.30 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0150]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal

oxidation at the 0.30 micrometer/min pan. Subsequently, SiO2 of a front face It lets a layer pass and is helium+. The 5x1016cm-2 ion implantation was carried out by 80keV(s).
[0151] This SiO2 Superposition, after making it contact, when the layer front face and the front face of Si substrate (the 2nd substrate) prepared independently were annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. Selective etching of the front face by the side of the 2nd base is carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0152] In this way, the single crystal Si layer which had the thickness of 0.2 micrometers on Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**6nm.
[0153] Furthermore, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0154] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0155] Moreover, selective etching is carried out, also agitating after that the ion-implantation layer which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0156] (Example 10) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.30 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0157]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.30 micrometer/min pan. SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 40keV(s).
[0158] This SiO2 The layer front face and the front face of Si substrate (the 2nd substrate) prepared independently were piled up, and were contacted.
[0159] A 1st substrate side to CO2 after removing the rear-face oxide film of the 1st substrate Laser was irradiated all over the wafer. CO2 Laser is 200nm SiO2 of a lamination interface. It was absorbed by the layer, and the temperature of the near rose rapidly and was separated into two sheets near the projection range of an ion implantation by the rapid thermal stress in an ion-implantation layer. Continuation or a pulse is also available for laser.
[0160] Selective etching of the front face by the side of the 2nd base was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0161] In this way, the single crystal Si layer which had the thickness of 0.2 micrometers on Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**6nm.
[0162] Furthermore, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0163] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0164] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.

[0165] (Example 11) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.30 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0166]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.30 micrometer/min pan. Subsequently, SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 40keV(s).
[0167] This SiO2 They are a layer front face and the front face of Si substrate (the 2nd substrate) prepared independently SiO2 of the lamination wafer end face superposition and after making it contact When the layer and the epitaxial Si layer were exfoliated by etching, ion-implantation **** appeared.
[0168] When 1000-degree C PAIRO oxidation was carried out, two substrates separated the lamination wafer completely in the ion-implantation layer in 10 hours. When the field which exfoliated was observed, the ion-implantation layer of the wafer periphery section is SiO2. Although it was changing, the center section was still origin mostly.
[0169] Then, selective etching was carried out, agitating the ion-implantation layer which remained in the 2nd substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0170] In this way, the single crystal Si layer which had the thickness of 0.2 micrometers on Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**6nm.
[0171] Furthermore, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0172] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0173] Moreover, selective etching is carried out, also agitating after that the ion-implantation layer which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0174] (Example 12) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.30 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0175]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.30 micrometer/min pan. SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 40keV(s).
[0176] this SiO2 the superposition after carrying out plasma treatment of a layer front face and the front face of Si substrate (the 2nd base) prepared independently and rinsing them -- it was made to contact Heat treatment of 300 degrees C - 1 hour was performed, and lamination reinforcement was raised. When the wedge was put in from the perimeter of a lamination substrate, it separated into two sheets near the projection range of an ion implantation. Since the ion-implantation layer has become porosity-like, it is ruined. Selective etching of the front face by the side of the 2nd base is carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0177] That is, the single crystal Si layer which had the thickness of 0.2 micrometers on Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**6nm.
[0178] Furthermore, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-

micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0179] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0180] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0181] (Example 13) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.30 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0182]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : It formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.30 micrometer/min pan. Next, SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 40keV(s).
[0183] this SiO2 the superposition after carrying out plasma treatment of a layer front face and the front face of Si substrate (the 2nd substrate) prepared independently and rinsing them -- it was made to contact Heat treatment of 300 degrees C - 1 hour was performed, and lamination reinforcement was raised. When shearing force was applied to the lamination substrate, it separated into two sheets near the projection range of an ion implantation. Selective etching of the front face by the side of the 2nd substrate was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0184] That is, the single crystal Si layer which had the thickness of 0.2 micrometers on Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**6nm.
[0185] Furthermore, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0186] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0187] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0188] When supplying as the 1st base again, it became reusable semipermanently by compensating a wafer thickness decrement with an epitaxial layer. That is, epitaxial thickness serves as a wafer thickness decrement instead of 0.30 micrometers 2nd after a repeat, and an ion-implantation layer is formed in the interior of an epitaxial layer.
[0189] (Example 14) It is H+ to the main front face on the 1st single crystal Si substrate. The 5x1016cm-2 ion implantation was carried out by 10keV(s). subsequently, CVD (Chemical Vapor Deposition) -- 0.30 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0190]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : In a 0.30 micrometer/min pan, it is 200nm SiO2 to this epitaxial Si layer front face. The layer was formed.
[0191] This SiO2 Superposition, after making it contact, when the layer front face and the front face of Si substrate (the 2nd substrate) prepared independently were annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. Since the ion-implantation layer has become porosity-like, it is ruined. Selective etching of the front face by the side of the 2nd substrate was carried

out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0192] Furthermore, the remainder of the 1st substrate equivalent to the ion-implantation depth was removed by etching.
[0193] In this way, the single crystal Si layer which had the thickness of 0.2 micrometers on Si oxide film has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**7nm.
[0194] Furthermore, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0195] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0196] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st base side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0197] (Example 15) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.50 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0198]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : At the time of 0.30 micrometer/min **, doping gas was added and it considered as n+Si/n-Si/Si substrate structure.
[0199] Furthermore, it formed 200nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation. Subsequently, SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 40keV(s).
[0200] This SiO2 Superposition, after making it contact, when the layer front face and the front face of Si substrate (the 2nd substrate) prepared independently were annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. Selective etching of the front face by the side of the 2nd substrate was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0201] In this way, n+ which had the thickness of 0.2 micrometers on Si oxide film The single crystal Si layer with an embedding layer has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 201nm**6nm.
[0202] Furthermore, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0203] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0204] Moreover, selective etching was carried out, also agitating after that the ion-implantation layer which remained in the 1st substrate side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0205] (Example 16) a 1st single crystal Si substrate top -- CVD (Chemical Vapor Deposition) -- 0.30 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0206]
Source gas: SiH2 Cl2 / H2 quantity of gas flow : 0.5 / 180 l/min gas pressure : 80Torr temperature : 950-degree-C growth rate : At the time of 0.30 micrometer/min **, doping gas was added and it considered

as n+Si/n-Si/Si substrate structure.
[0207] Furthermore, it is 50nm SiO2 by thermal oxidation to this epitaxial Si layer front face. The layer was formed. SiO2 of a front face It lets a layer pass and is H+. The 5x1016cm-2 ion implantation was carried out by 40keV(s).
[0208] This SiO2 A layer front face and 500nm SiO2 prepared independently Superposition, after making it contact, when the front face of Si substrate (the 2nd base) in which the layer was formed was annealed at 600 degrees C, it separated into two sheets near the projection range of an ion implantation. Selective etching of the front face by the side of the 2nd base was carried out agitating with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the ion-implantation layer was carried out, and the single crystal Si was removed completely.
[0209] In this way, n+ which had the thickness of 0.29 micrometers on Si oxide film The single crystal Si layer with an embedding layer has been formed. When 100 points were measured for the thickness of the formed single crystal Si layer about the whole surface within a field, the homogeneity of thickness was 291nm**9nm.
[0210] Furthermore, it heat-treated at 1100 degrees C in hydrogen for 1 hour. When the atomic force microscope estimated surface roughness, the 2nd [an average of] power granularity in the field of 50-micrometer angle was equivalent to Si wafer usually marketed by about 0.2nm.
[0211] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0212] Moreover, selective etching is carried out, also agitating after that the ion-implantation layer which remained in the 1st base side with the mixed liquor of fluoric acid and 30% hydrogen peroxide solution 49%. Then, surface treatment, such as hydrogen annealing or surface polish, was able to be performed, and it was able to supply as the 2nd base as the 1st base again.
[0213] (Example 17) About the above-mentioned examples 1-16, the same processing as both sides of the 1st base was performed, and the semi-conductor member was obtained.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is a typical sectional view for explaining the process of the example 1 of an embodiment of this invention.
[Drawing 2] It is a typical sectional view for explaining the process of the example 2 of an embodiment of this invention.
[Drawing 3] It is a typical sectional view for explaining the process of the example 3 of an embodiment of this invention.
[Drawing 4] It is a typical sectional view for explaining the process of the 1st conventional example.
[Drawing 5] It is a typical sectional view for explaining the process of the 2nd conventional example.
[Description of Notations]
11 1st Si Single Crystal Substrate
12 Nonvesicular Layer
13 Insulating Layer
14 Collect Ion Notes ON.
15 2nd Substrate

[Translation done.]

* NOTICES *

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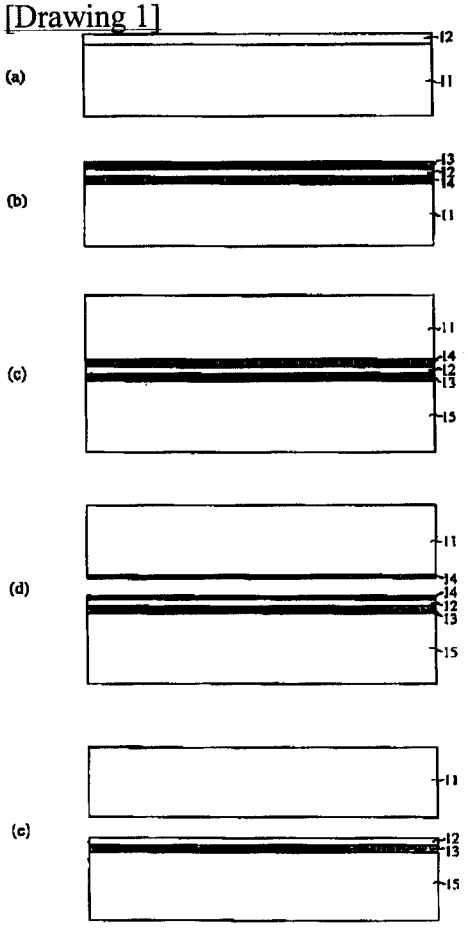
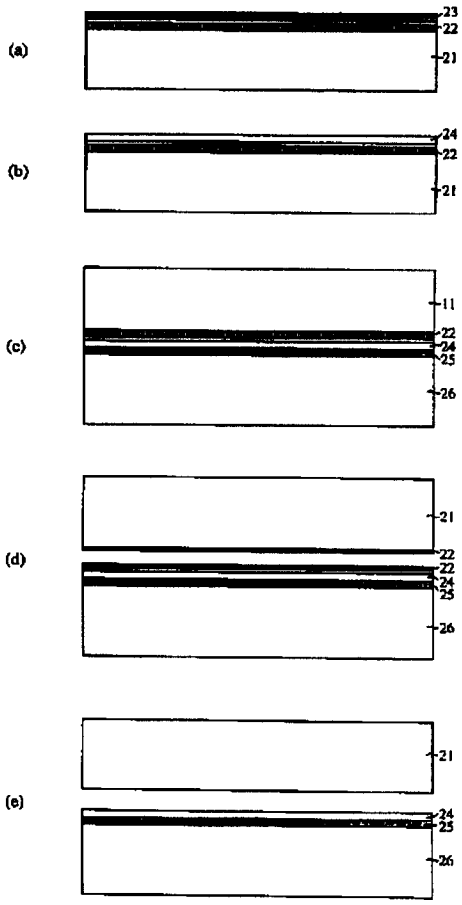
DRAWINGS

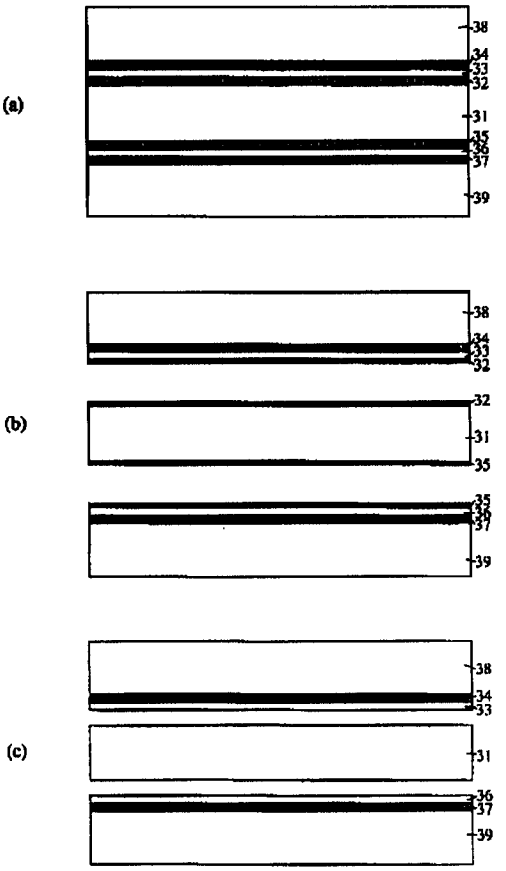
[Drawing 1]



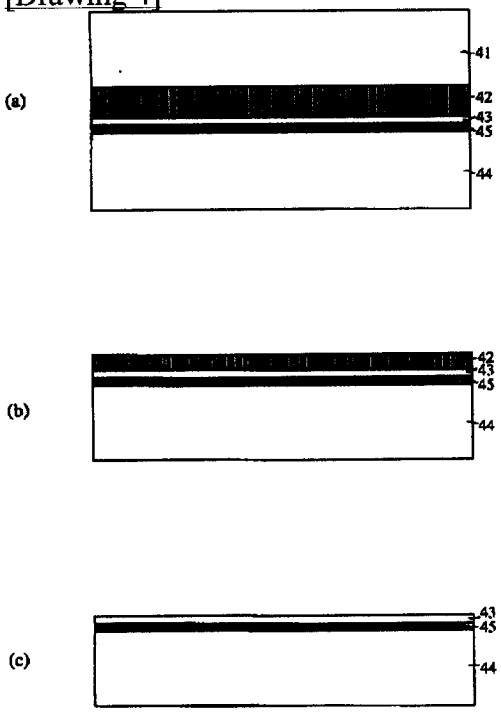
[Drawing 2]



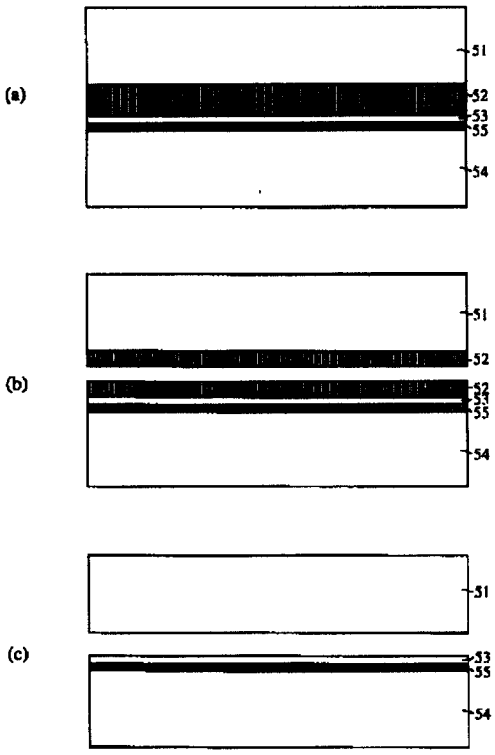
[Drawing 3]



[Drawing 4]



[Drawing 5]



[Translation done.]